



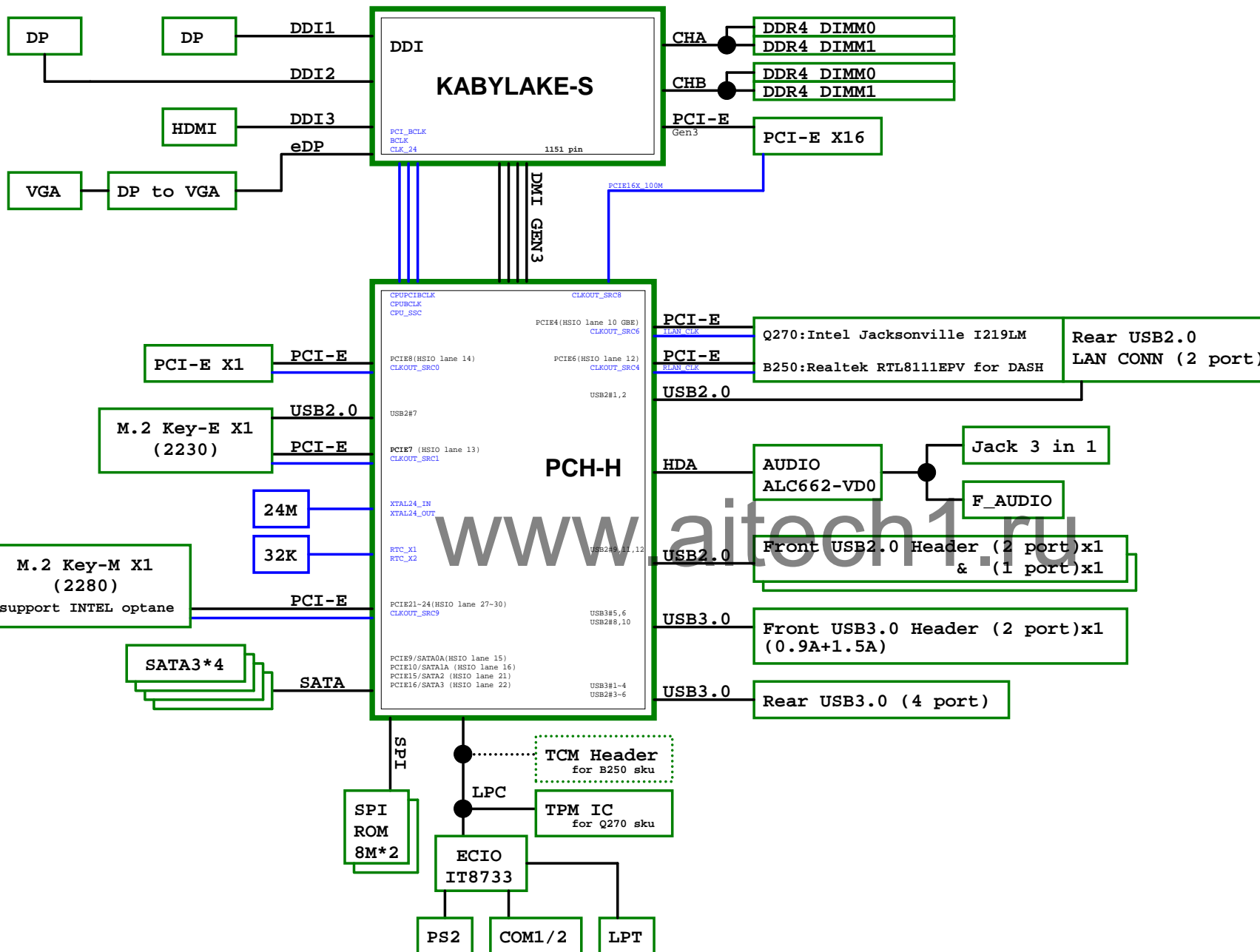
Q27H4-AD

Rev:1.0

ECS
CONFIDENTIAL

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PCH-GPIO function

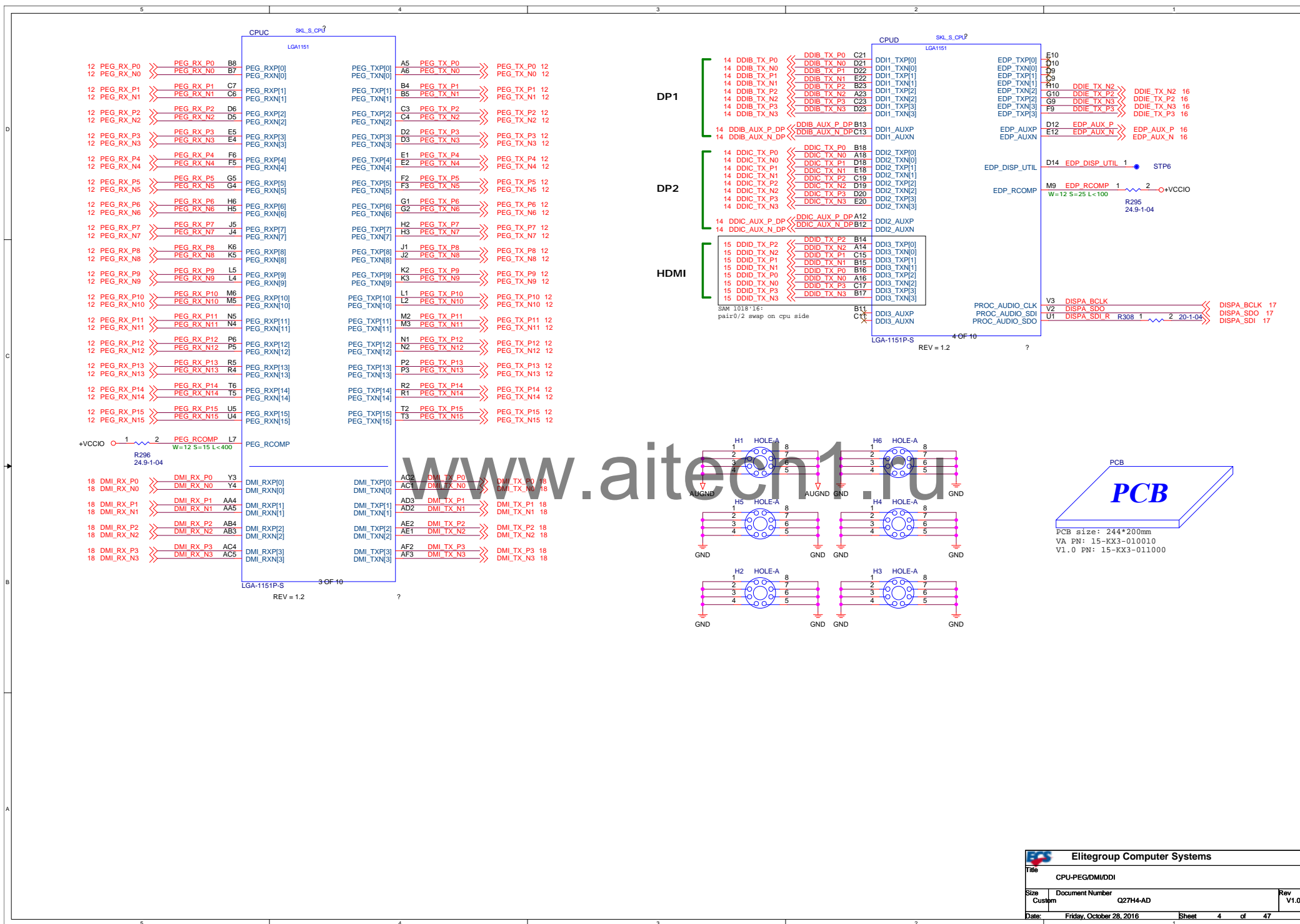
Pin Name	Power Well	Usage	Default Status
GPP_D7	3VSB	GPP_D7_CASEOPEN (reserved)	GPIO(GPI)
GPP_D6	3VSB	GPP_D6_BIOSWP	GPIO(GPI)
GPP_D5	3VSB	GPP_D5_BIOS_WP	GPIO(GPI)
GPD10	ATX_3VSB	GPD10 (ME disable by SW)	SLP_S5#
GPD2	ATX_3VSB	ILAN_WAKE_L	LAN_WAKE#
GPD0	ATX_3VSB	RLAN_PWR_EN (only for B25 sku)	BATLOW#
GPD11	ATX_3VSB	LAN_DIS_L	LANPHYPC
GPP_A12	3VSB	GPP_A12_TPM H:with on-board TPM L:W/O on-board TPM	GPIO(GPI)
GPP_A11	3VSB	LPC_PME_L	PME#
GPP_G13	VCC3	HDPANEL_DETECT (reserved)	GPIO(GPI)
GPP_A14	VCC3	LPCPD_L	SUS_STAT#
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A5	N/A	LPC_FRAME_L	LFRAME#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	TCM_TPM_24M	CLKOUT_LPC1
GPP_B3	VCC3	BT_DISABLE_L L:disable	GPIO(GPI)
GPP_B17	VCC3	WLAN_DISABLE_L L:disable	GPIO(GPI)
GPP_E8	VCC3	SATALED_L	SATA_LED#
GPP_F16	3VSB	GPP_F16 H: USB power enable	GPIO(GPI)
GPP_I0	N/A	DDPB_HPD0	DDPB_HPD0
GPP_I1	N/A	DDPC_HPD1	DDPC_HPD1
GPP_I2	N/A	DDPD_HPD2	DDPD_HPD2
GPP_I2	N/A	DDPE_HPD3	DDPE_HPD3
GPP_G23	3VSB	GPP_G22 H:default BIOS L:on-board VGA	GPIO(GPI)
GPP_F22	VCC3	GPP_F22_PCIEIRST (PCIEx16 SW RST#)	GPIO(GPI)
GPD9	ATX_3VSB	PCH_RI_L L:RI# wake up	SLP_WLAN#
GPP_H0	3VSB	ILAN_CLKREQ	SRCCCLKREQ6#
GPP_B6	3VSB	M2CLK_REQ1_L	SRCCCLKREQ1#
GPP_E0	3VSB	GPP_E0_OBR (ACER's OBR)	GPIO(GPI)
GPP_H14	3VSB	GPP_H14 (ACER reserved GPIO)	GPIO(GPI)
GPP_H15	3VSB	GPP_H15 (ACER reserved GPIO)	GPIO(GPI)
GPP_D1	+DIMM_5VDUAL	SIO_LED1	GPIO(GPI)
GPP_D0	+DIMM_5VDUAL	SIO_LED0	GPIO(GPI)

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	3VSB	basic health function	5VSB_CTRL#(DOD8)
GP31	3VSB	EC sleep mode wake up	PWNOUT(DOD8)
GP41	3VSB	GPP_E7_THERM (ACER's SW thermal shutdown)	FAN_CTL3(DOD8)
GP17,GP35	3VSB	VGA Wake up by Monitor (EC control)	
GP36,GP37	3VSB	HDMI Wake up by Monitor (EC control)	
GP34	3VSB	DP2 Wake up by Monitor (EC control)	
GP33	3VSB	DP1 Wake up by Monitor (EC control)	

CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5/6	CFG[2]:1 = Normal operation CFG[6:5]:1 = 1 x16 PCI Express	PCIEX6
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	0 = Enable
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lines.	
SPKR/GPP_B14	Top Swap Override	0 = Enable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 = Enable "No Reboot" mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit HBS	0 = SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 = LPC is selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.



DDR4 CH.A

9 M_DATA_A[0..63] << M_DATA_A[0..63]
 9 M_CLK_A_P[0..3] << M_CLK_A_P[0..3]
 9 M_CLK_A_N[0..3] << M_CLK_A_N[0..3]
 9 M_CKE_A[0..3] << M_CKE_A[0..3]
 9 M_CS_A_L[0..3] << M_CS_A_L[0..3]
 9 M_ODT_A[0..3] << M_ODT_A[0..3]
 9 M_MA_A[0..15] << M_MA_A[0..15]
 9 M_DQS_A_P[0..7] << M_DQS_A_P[0..7]
 9 M_DQS_A_N[0..7] << M_DQS_A_N[0..7]

DDR4 CH.B

10 M_DATA_B[0..63] << M_DATA_B[0..63]
 10 M_CLK_B_P[0..3] << M_CLK_B_P[0..3]
 10 M_CLK_B_N[0..3] << M_CLK_B_N[0..3]
 10 M_CKE_B[0..3] << M_CKE_B[0..3]
 10 M_CS_B_L[0..3] << M_CS_B_L[0..3]
 10 M_ODT_B[0..3] << M_ODT_B[0..3]
 10 M_MA_B[0..15] << M_MA_B[0..15]
 10 M_DQS_B_P[0..7] << M_DQS_B_P[0..7]
 10 M_DQS_B_N[0..7] << M_DQS_B_N[0..7]

9 M_DATA_A_CBK << M_DATA_A_CBK
 9 M_DATA_A_CBA << M_DATA_A_CBA
 9 M_DATA_A_CBB << M_DATA_A_CBB
 9 M_DATA_A_CBC << M_DATA_A_CBC
 9 M_DATA_A_CBD << M_DATA_A_CBD
 9 M_DATA_A_CBE << M_DATA_A_CBE
 9 M_DATA_A_CBF << M_DATA_A_CBF
 9 M_DATA_A_CBG << M_DATA_A_CBG

CPUA SKL_S_CP9
 LGA1151

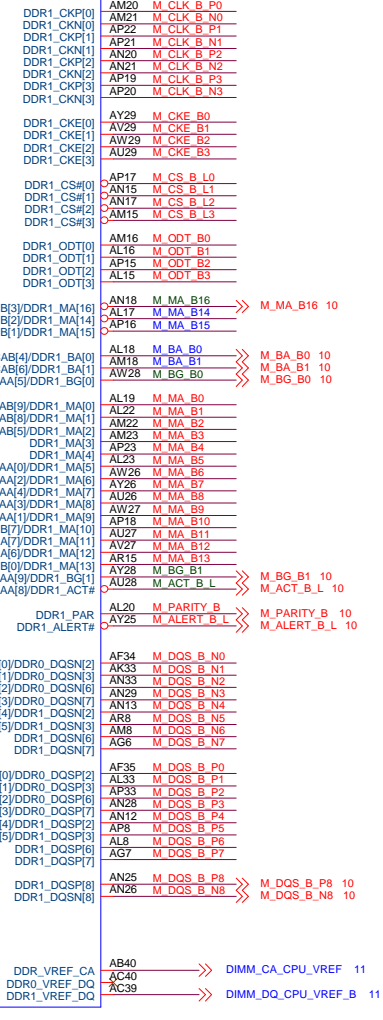


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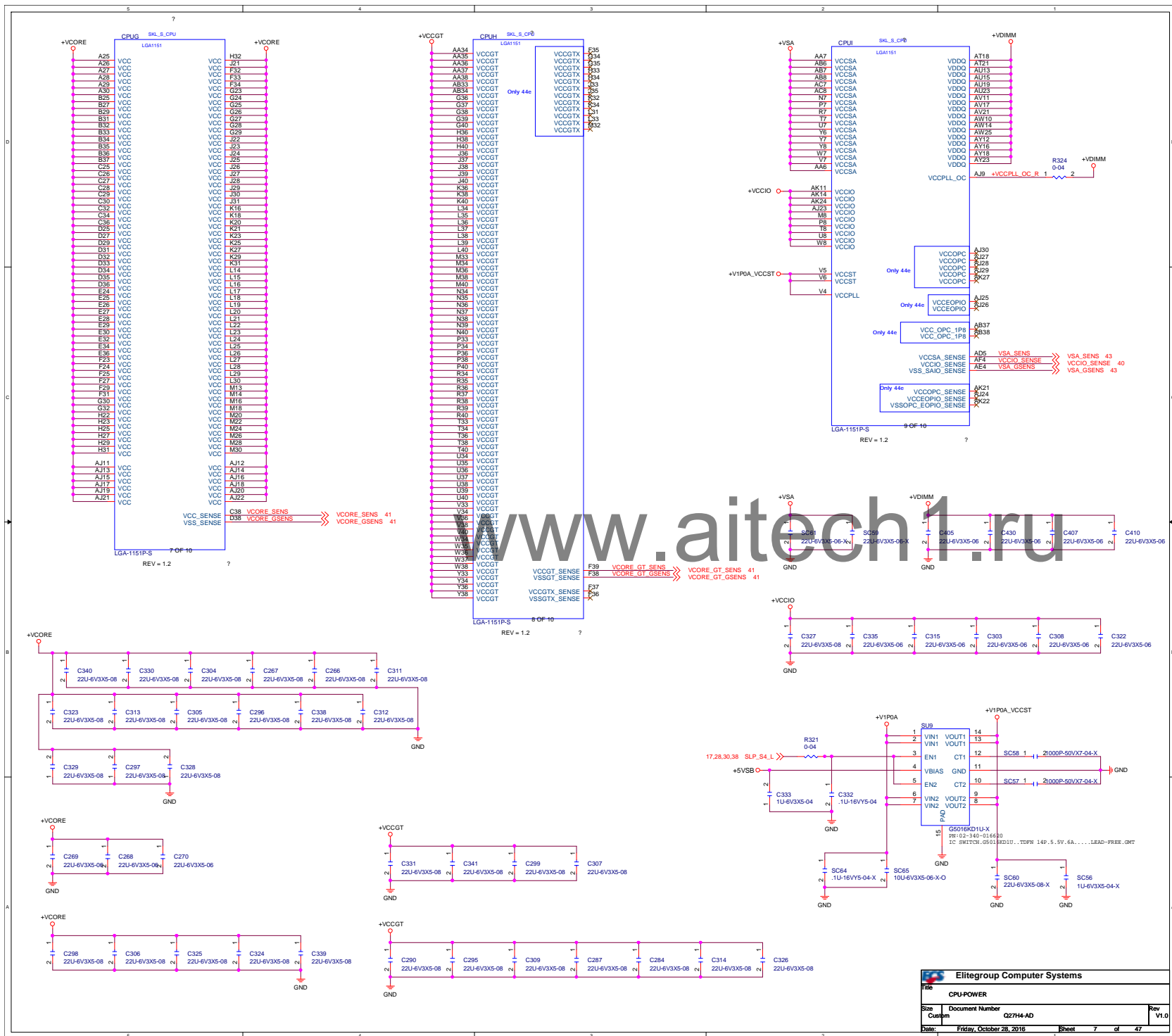
CPUB SKL_S_CP9
 LGA1151

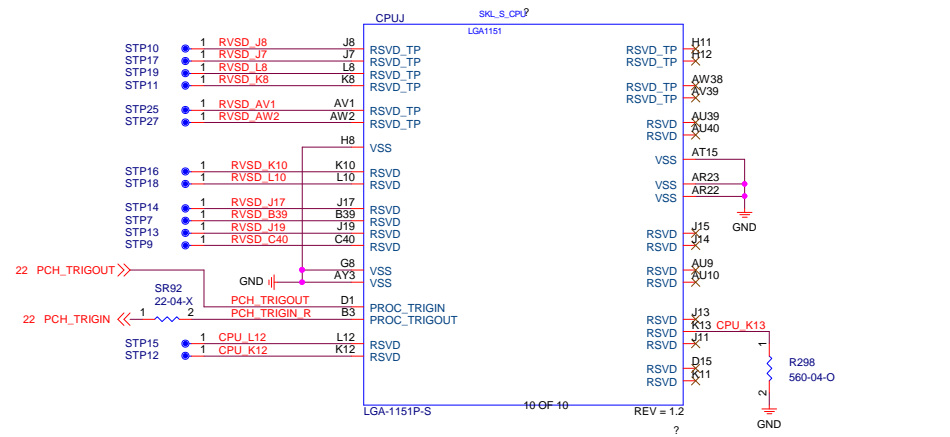


LGA-1151P-S REV = 1.2




LGA-1151P-S REV = 1.2

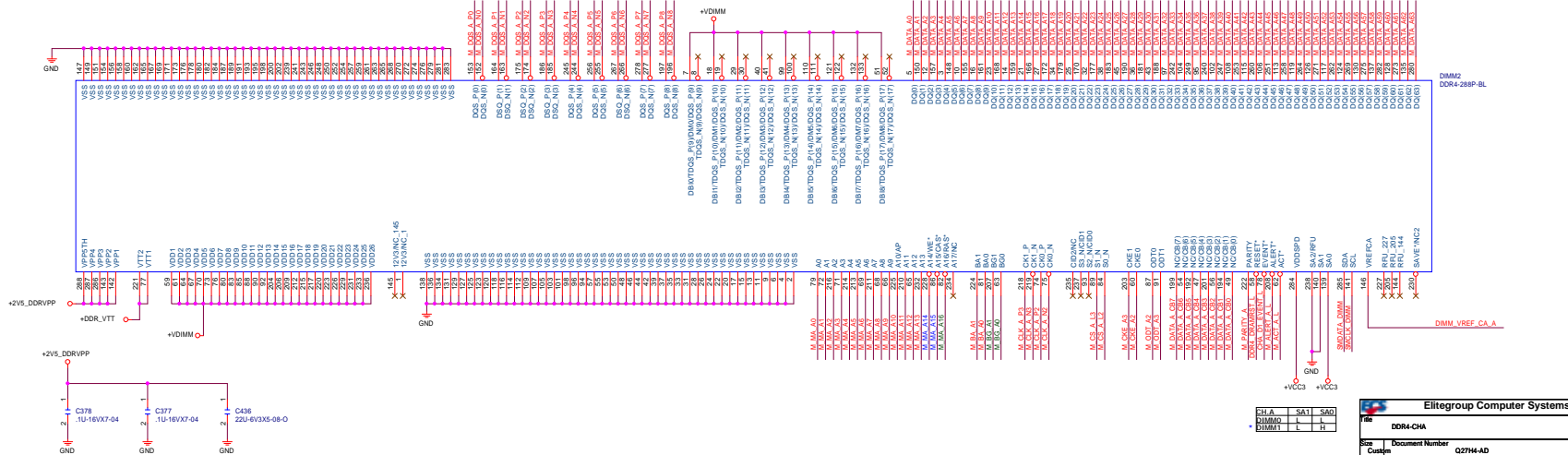
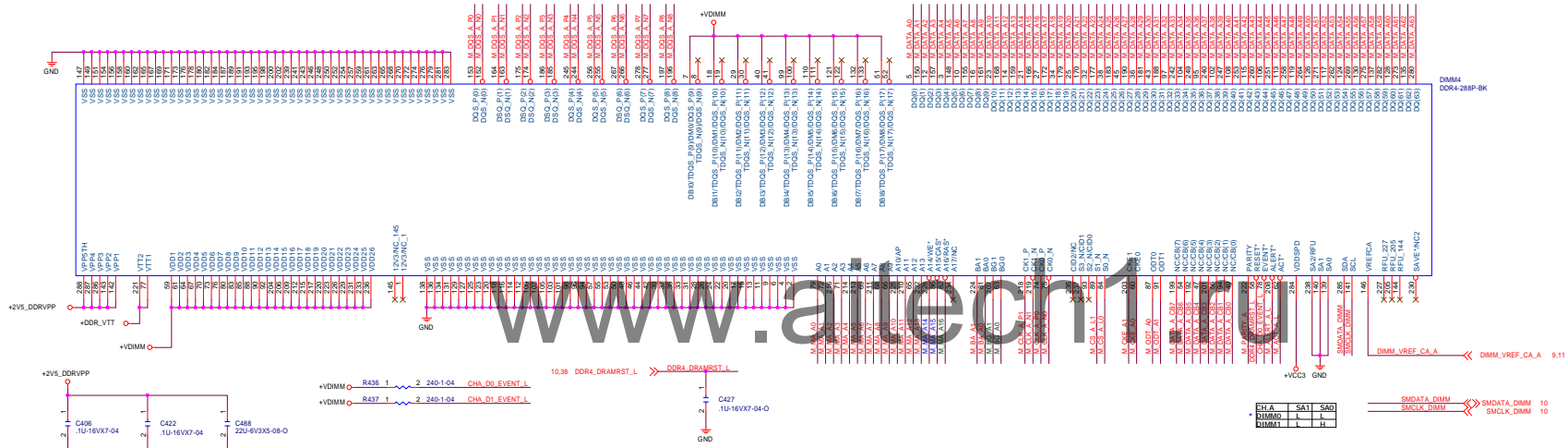
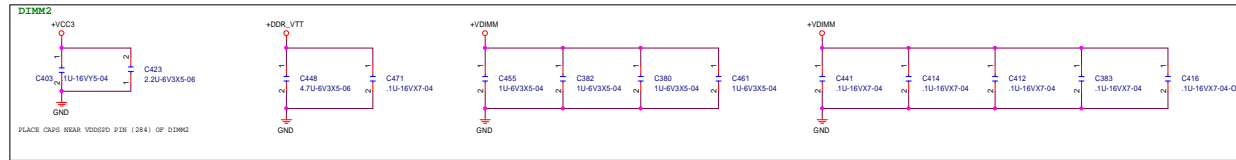
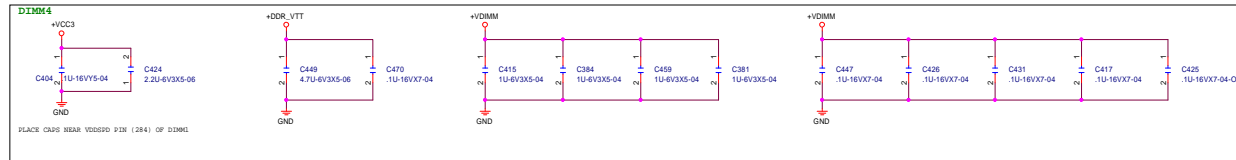
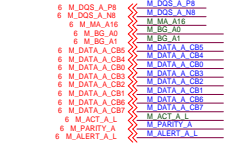
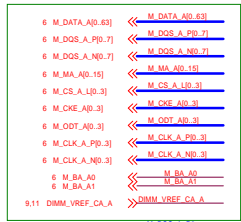




SAM 0901'16:
modify reference from CPU1 to CPU0


CPU
CPU_SUBASSY_STEEL

 Elitegroup Computer Systems			
Title CPU-GND			
Size Custom	Document Number Q27H4-AD		Rev V1.0
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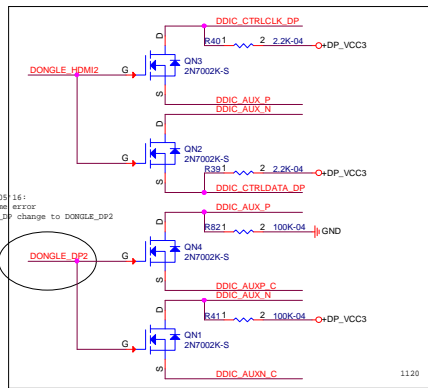
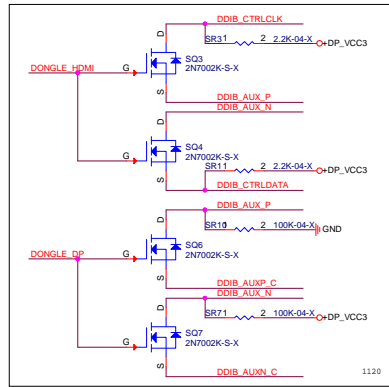




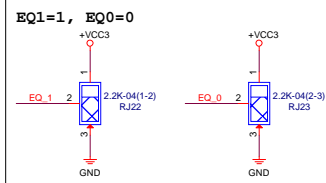
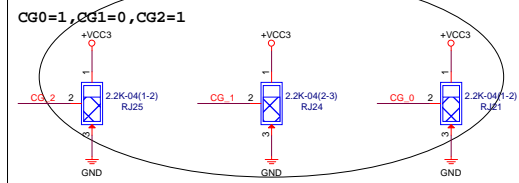
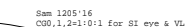
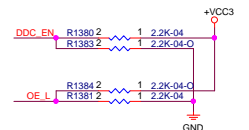
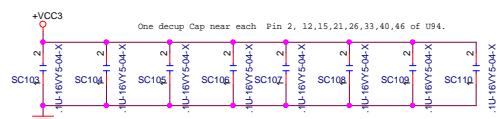
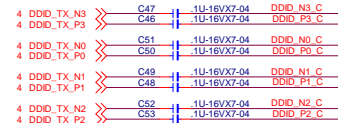
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Size Custom	Document Number Q27H4-AD
Date: Friday, October 28, 2016	Rev V1.0
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DP1
DP2



HDMI

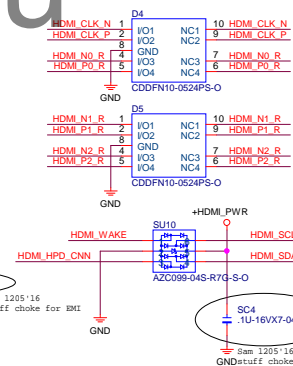
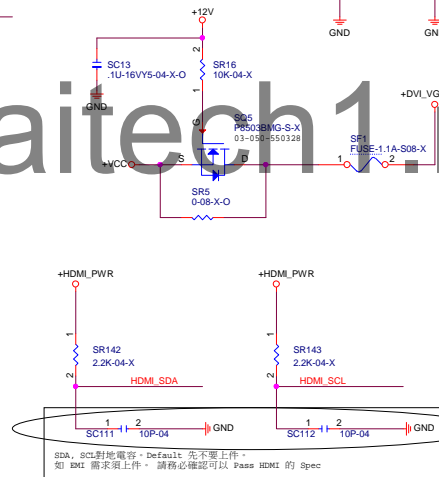
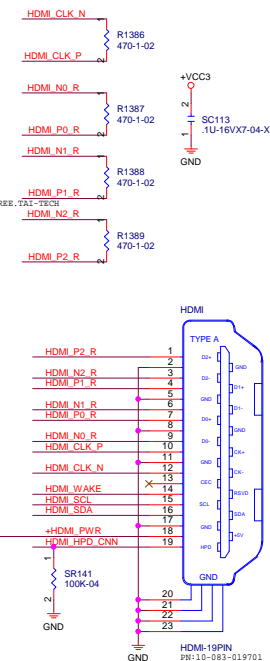
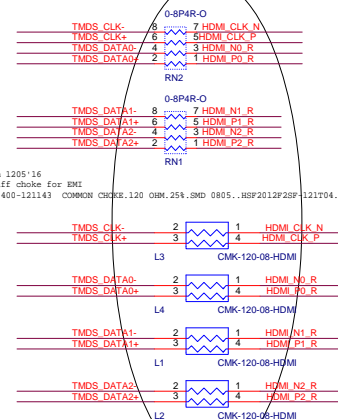
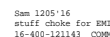
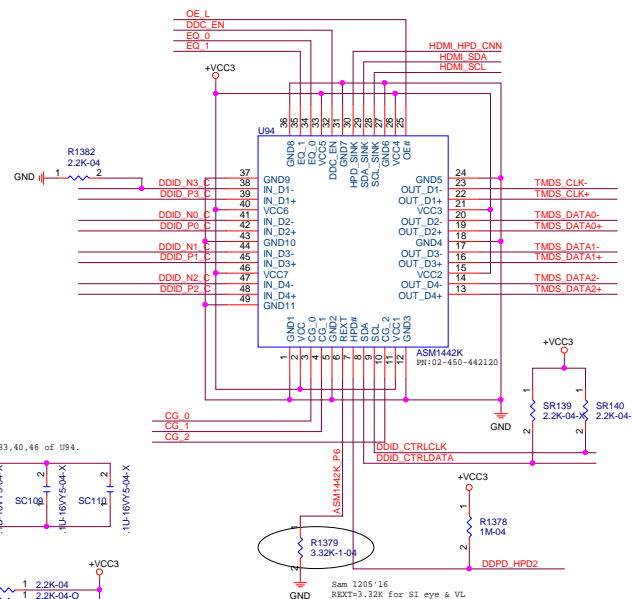


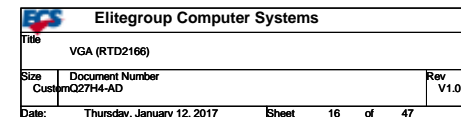
TMDS Input Signal Equalization

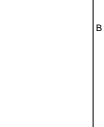
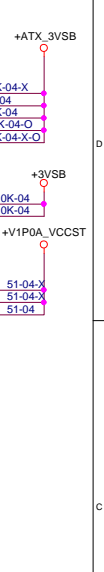
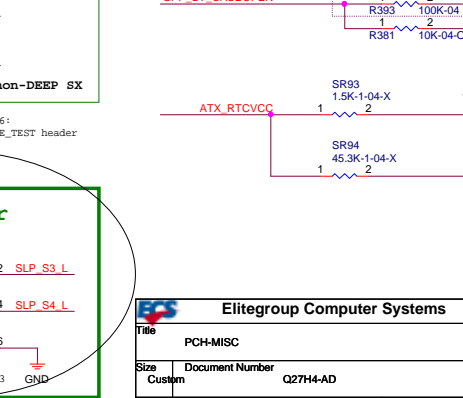
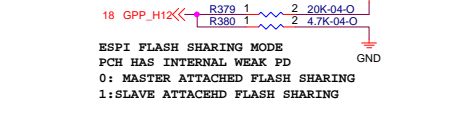
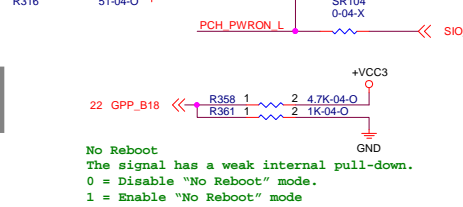
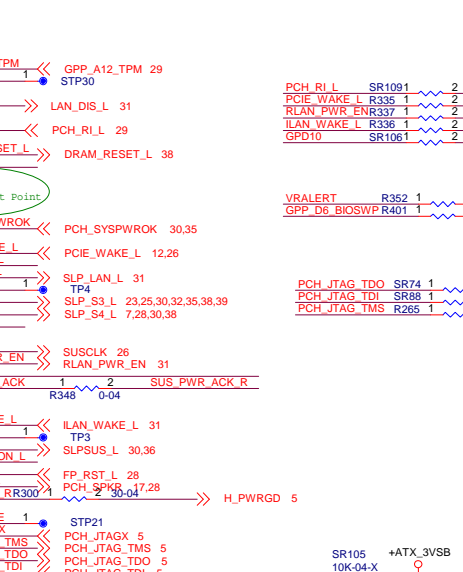
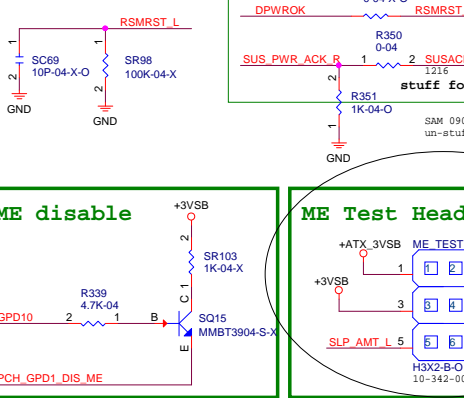
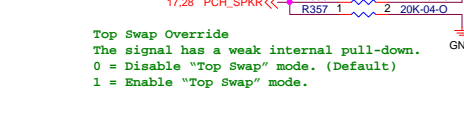
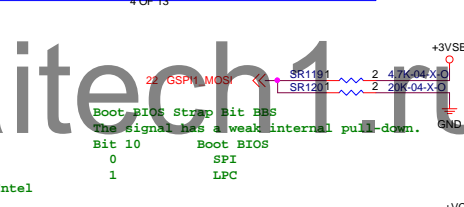
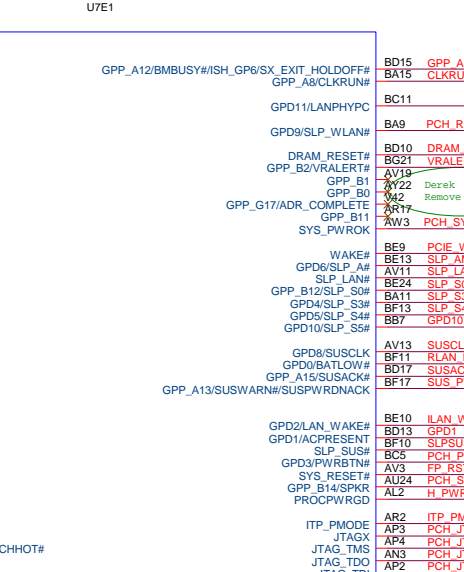
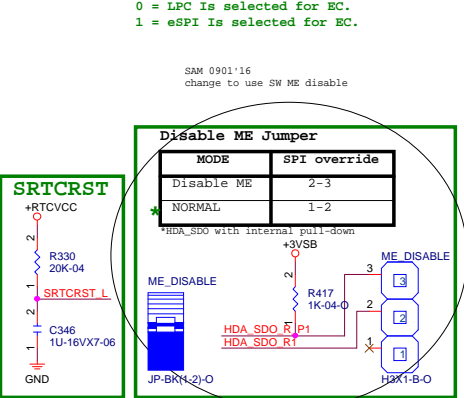
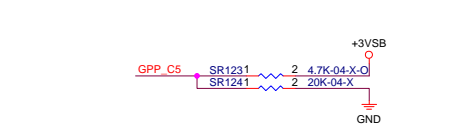
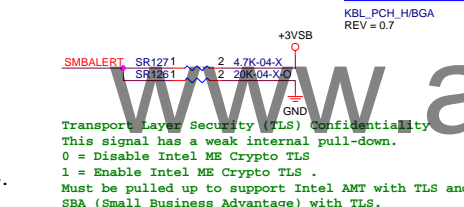
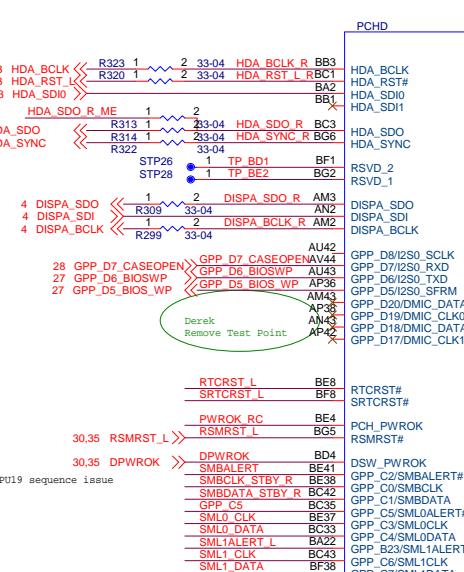
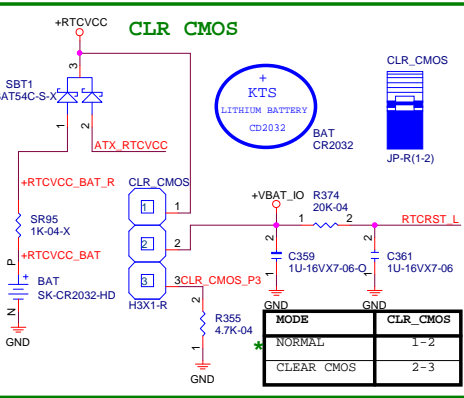
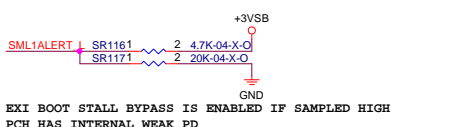
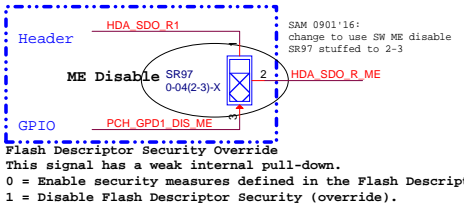
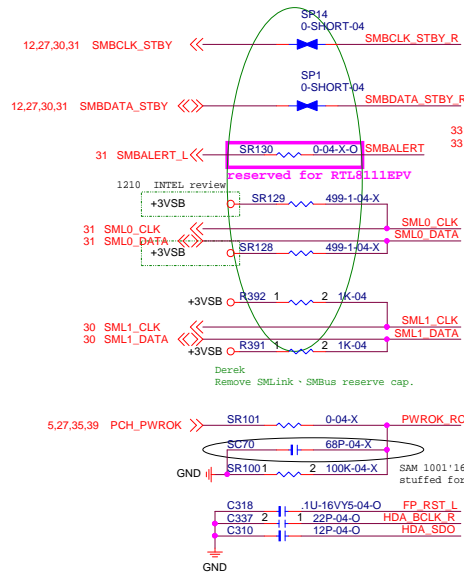
EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	3dB	
1	0	1dB	default
1	1	0dB	

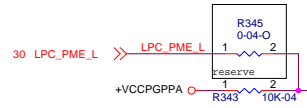
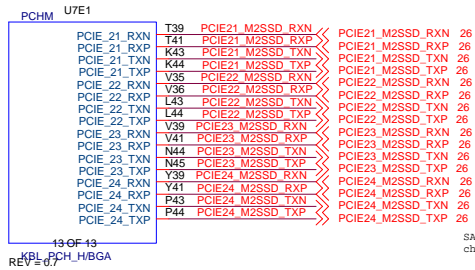
TMD5 Output Signal Integrity

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	453	0	0	
0	0	1	458	0	-0.66dB	
0	1	0	461	0	-1.60dB	Default
0	1	1	465	0	-0.66dB	
1	0	0	473	0	-1.60dB	
1	0	1	430	0.3dB	0	
1	1	0	425	0.3dB	0	
1	1	1	455	0	0	









integrated Pull up 15K-40K



SAM 1021:16:
change front panel LED control by PCH GPP_D0/D1

PCBA

GPP_A11/PME#

BF15

AH16

RSVD_18

RSVD_19

RSVD_20

RSVD_21

AU19

AP17

TP2

TP1

SPI0_MOSI

SPI0_MISO

SPI0_CS0#

SPI0_CLK

SPI0_CS1#

SPI0_IO2

SPI0_IO3

SPI0_CS2#

GPP_D1/SPH1_CLK

GPP_D0/SPH1_CS#

GPP_D3/SPH1_MOSI

GPP_D2/SPH1_MISO

GPP_D22/SPH1_IO3

GPP_D21/SPH1_IO2

INTRUDER#

BD24

T43

AC39

Y36

Y43

Y44

AP41

EXTTS_SNI_DRV0_PCH

AK43

GPP_E7_THERM

BT_DISABLE_L

BF22

EXTTS_SNI_DRV1_PCH

GPP_H18

BF34

GPP_H17/SML4ALERT#

GPP_H16/SML4CLK

GPP_H15/SML3ALERT#

GPP_H14/SML3DATA

GPP_H13/SML3CLK

GPP_H12/SML2ALERT#

GPP_H11/SML2DATA

GPP_H10/SML2CLK

INTRUDER#

BF9

PCH_INTRUDER_L

1

RTCVCC

2

10K-04

1

RTCVCC

2

10K-04

1

RTCVCC

2

10K-04

1

RTCVCC

2

10K-04

1

RTCVCC

2

10K-04

1

RTCVCC

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10K-04

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RTCVCC

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10K-04

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RTCVCC

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RTCVCC

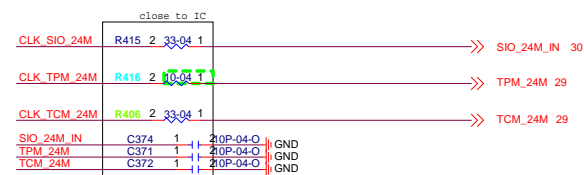
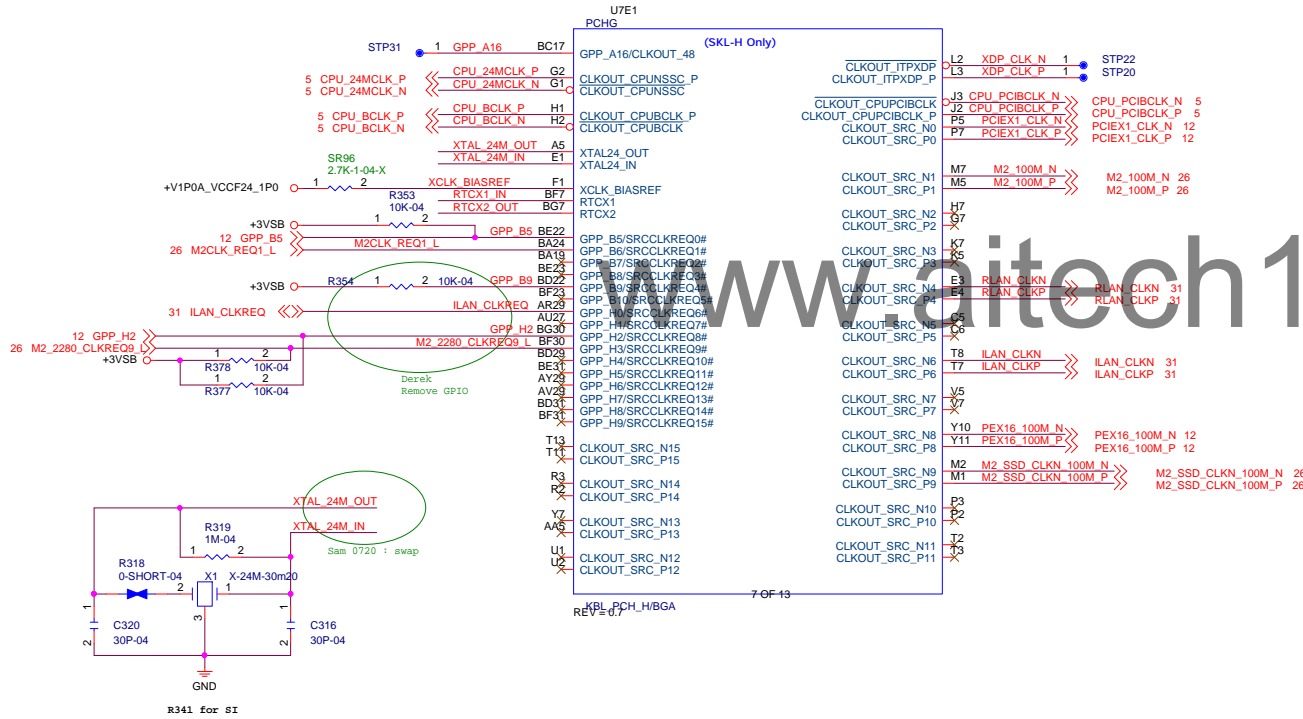
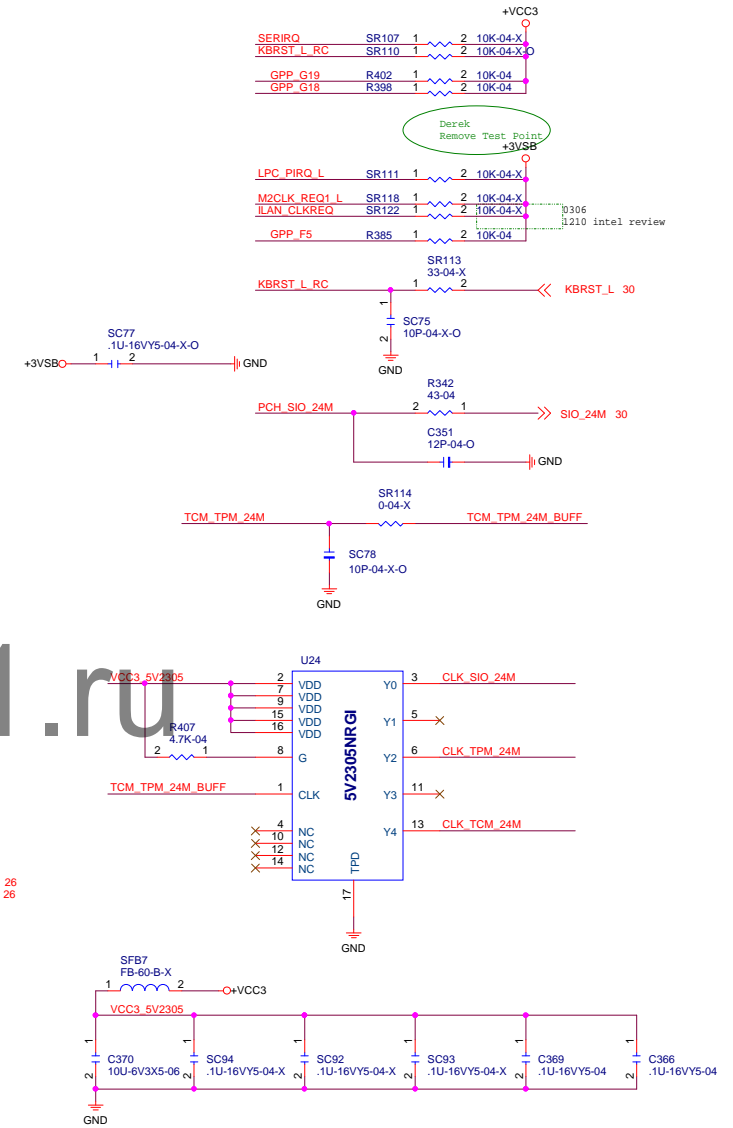
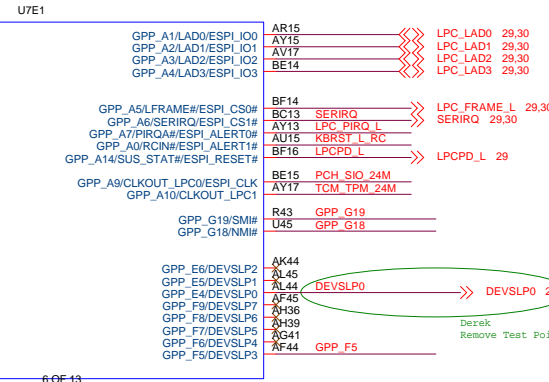
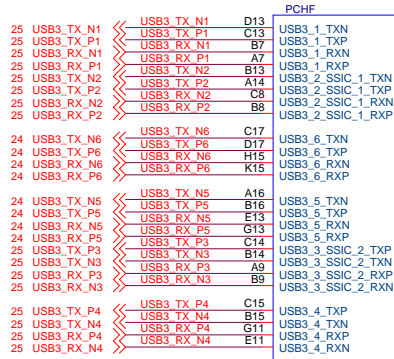
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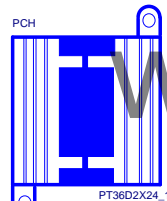
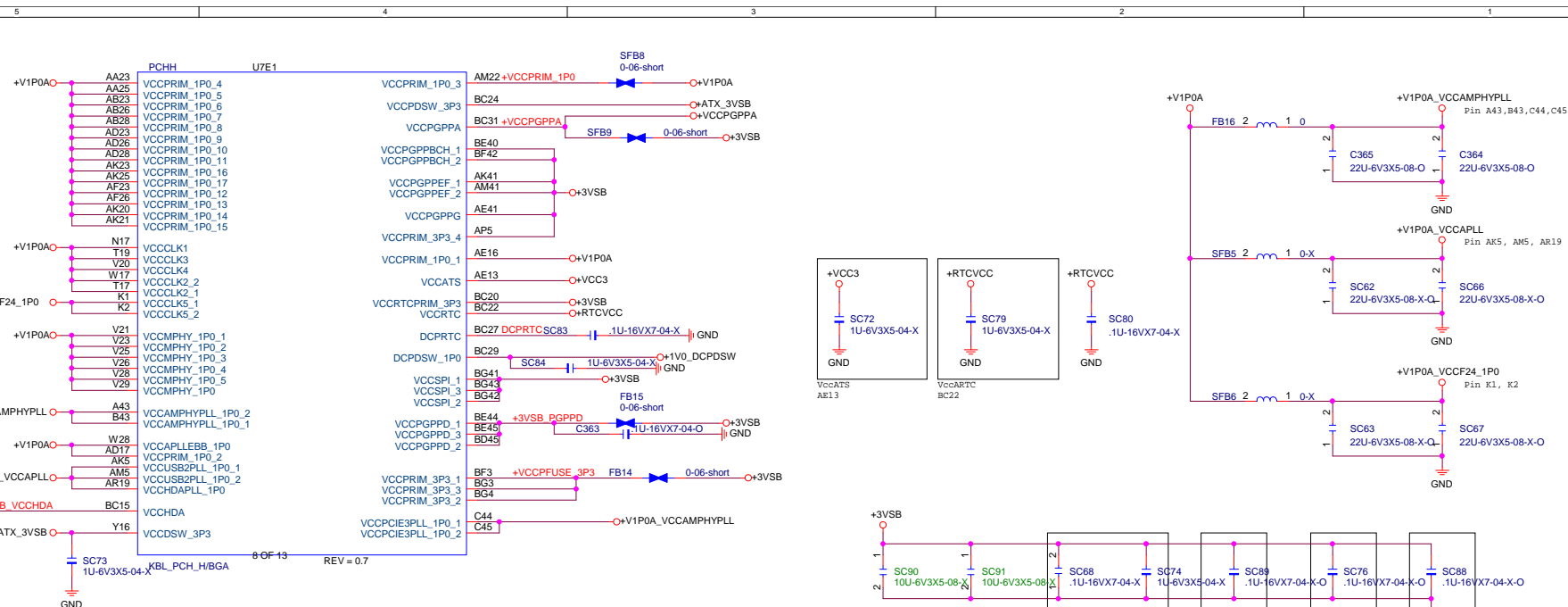
10K-04

Rear IO USB3.0

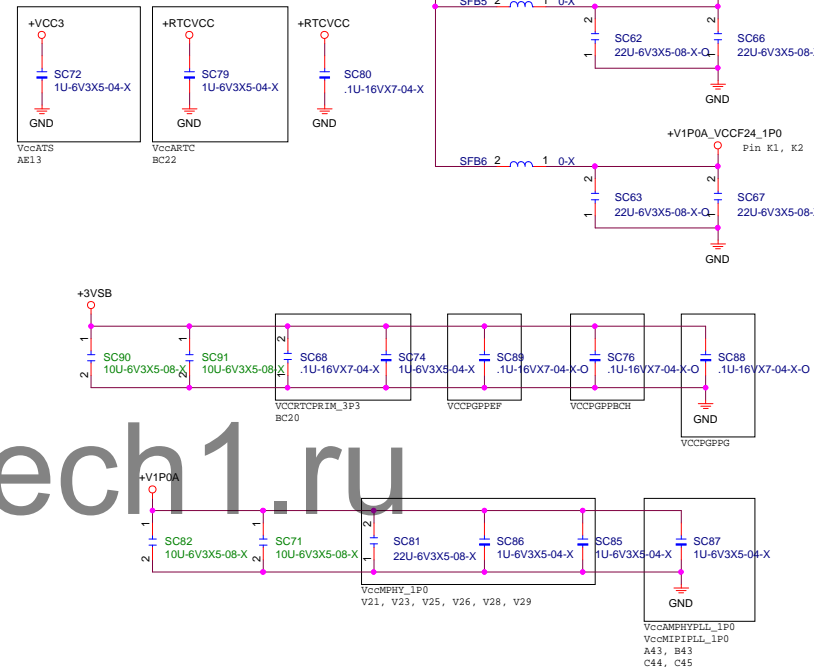
Front IO USB3.0

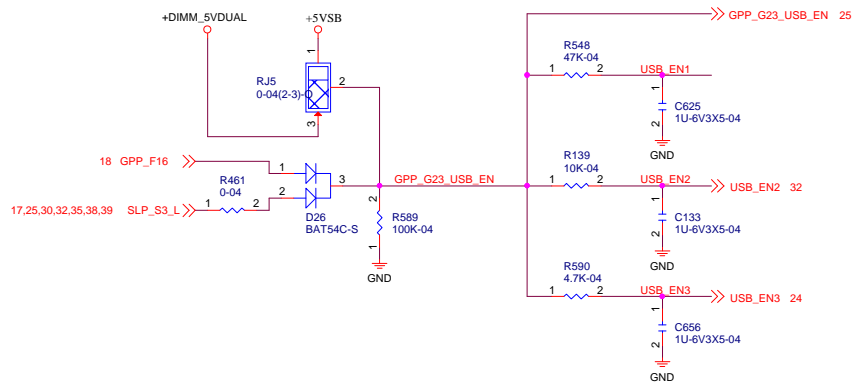
Rear IO USB3.0





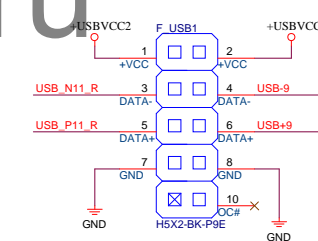
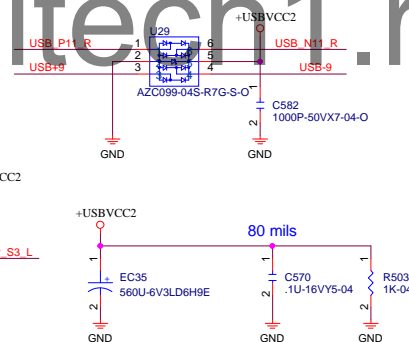
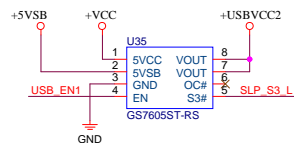
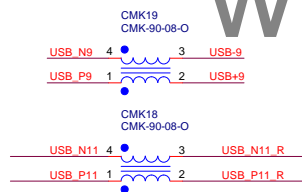
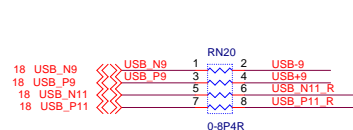
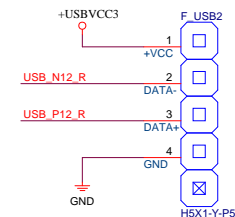
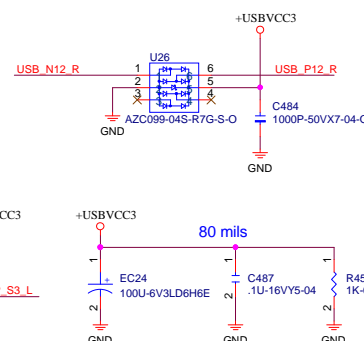
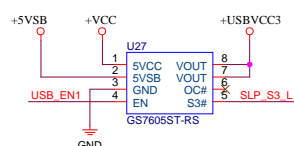
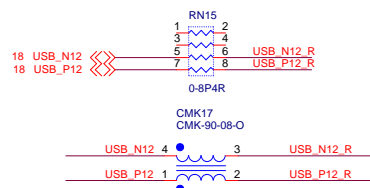
PCH heatsink (T/U phase)
P/N:20-120-013584
HEAT SINK...SILVER.RHS04441R0.SB.31.5*31*1.5mm....
W/PUSH PIN*2,PAD,FOAM....LEAD-FREEE(RoHS/HF).ZHIHANG



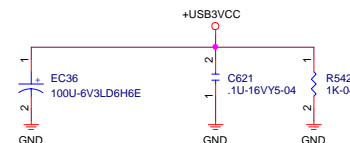
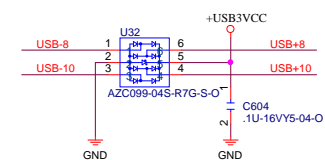
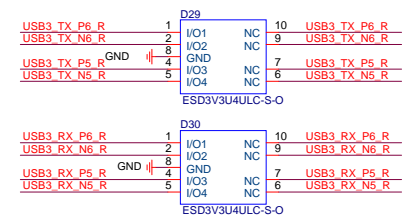
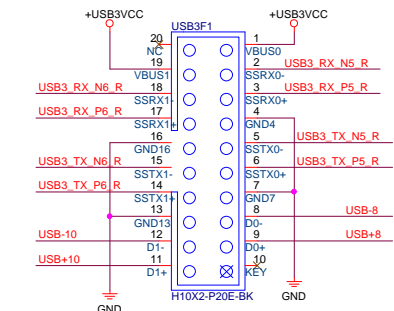
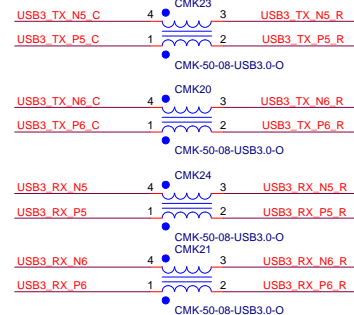


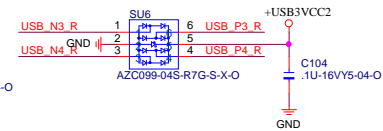
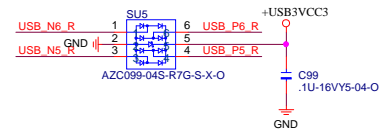
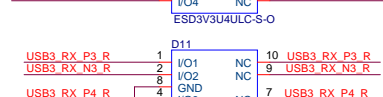
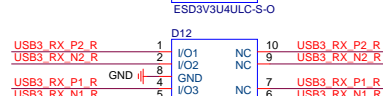
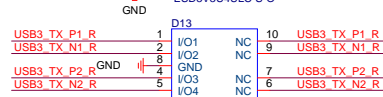
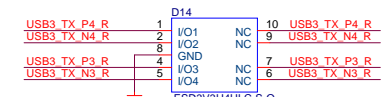
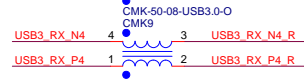
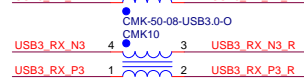
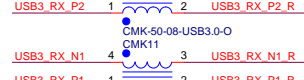
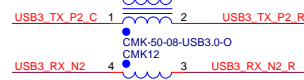
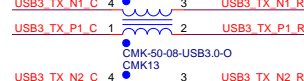
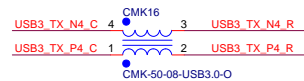
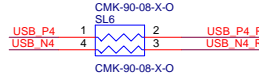
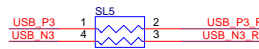
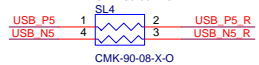
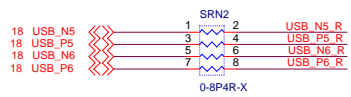
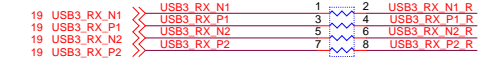
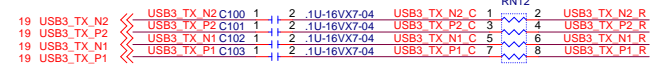
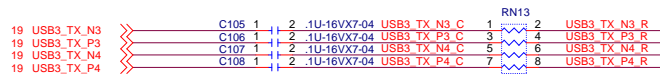
	power switch Enable use	RJ5	D62	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB_PWR	ON	ON	ON	OFF

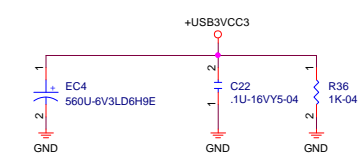
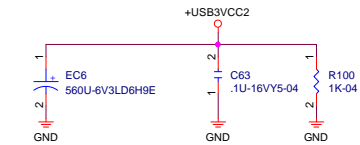
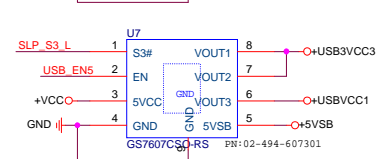
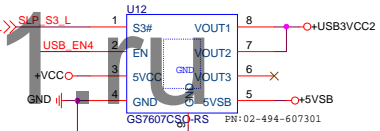
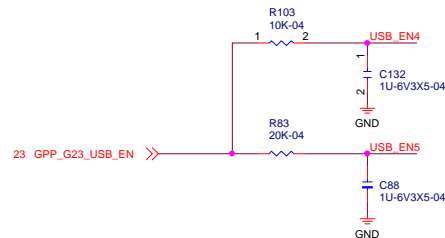


www.aitech1.ru

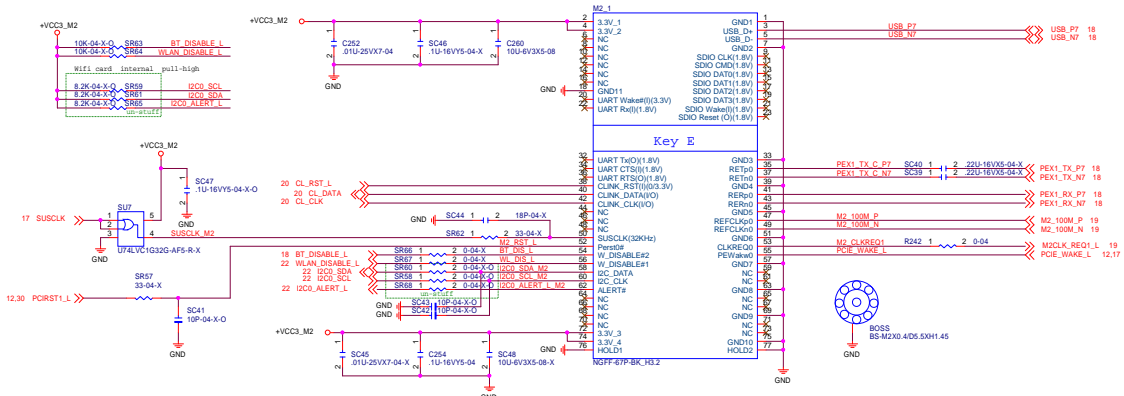




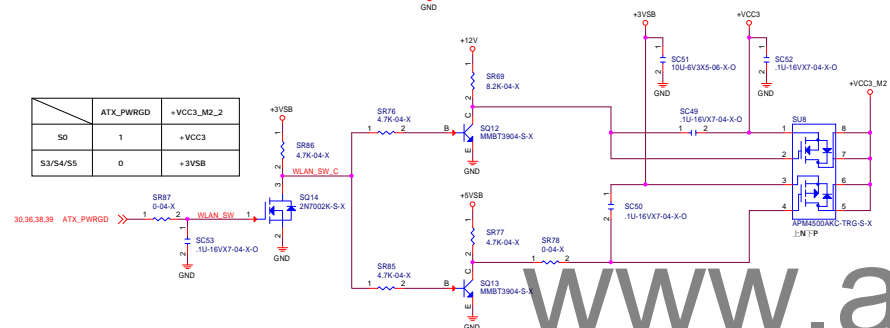
www.aitech1.ru



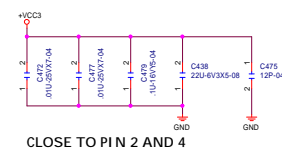
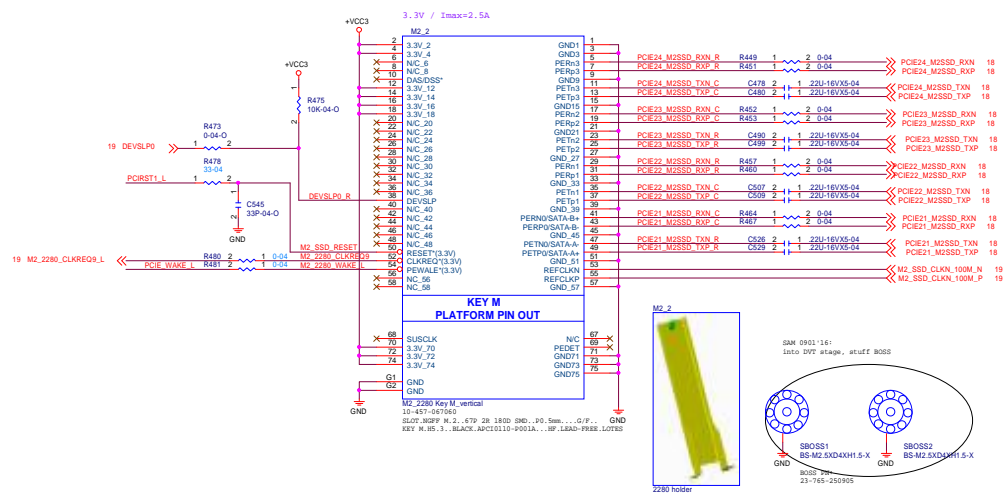
M.2 WIFI



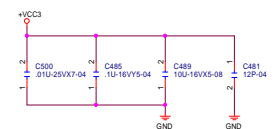
	ATX_PWRGD	+VCC3_M2_2
S0	1	+VCC3
S3/S4/S5	0	+3VSB



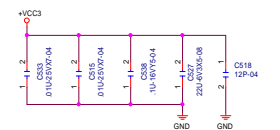
M.2 SSD



CLOSE TO PIN 2 AND 4

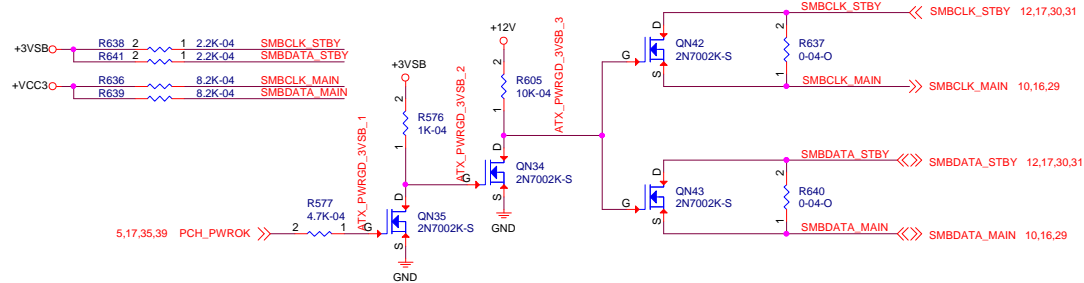


CLOSE TO PIN 12,14,16 AND 18

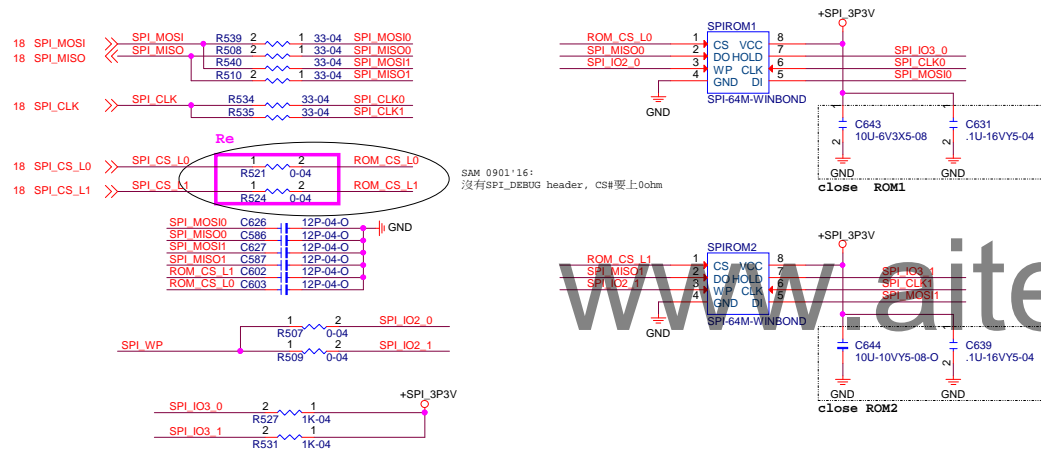


CLOSE TO PIN 70 72 AND 74

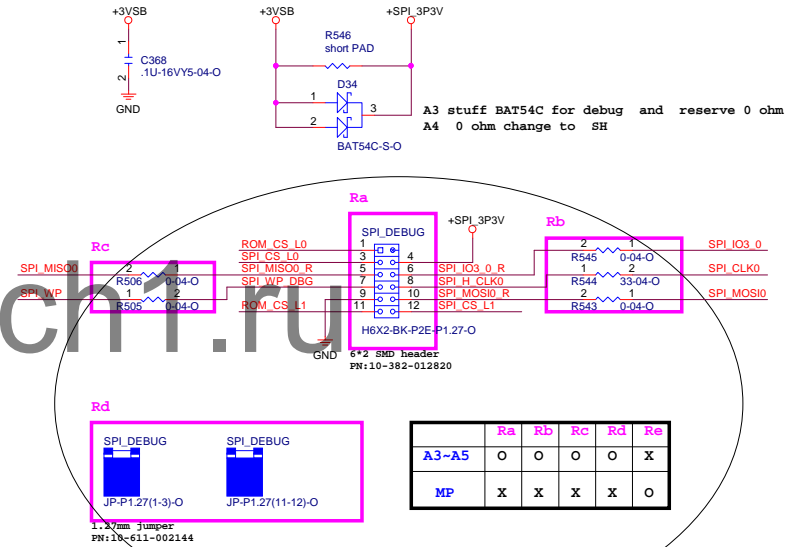
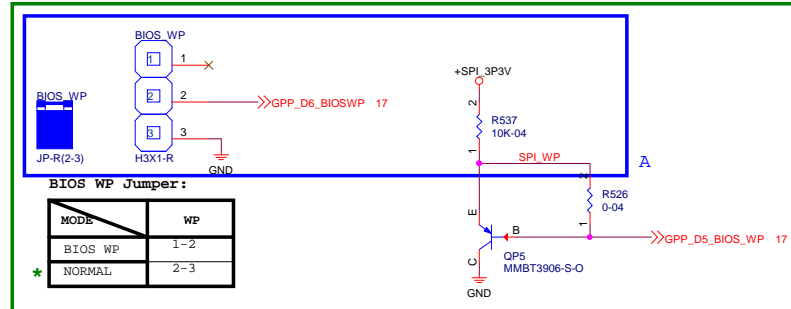
SMbus Logic Circuit



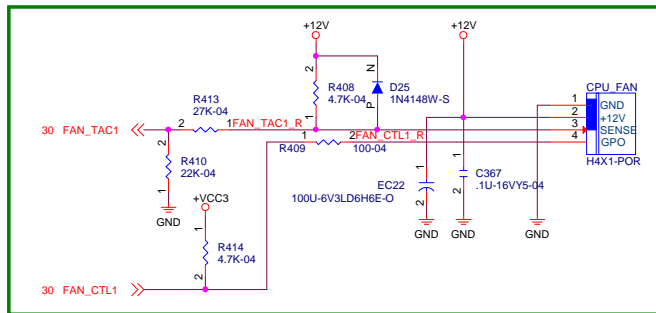
SPI ROM



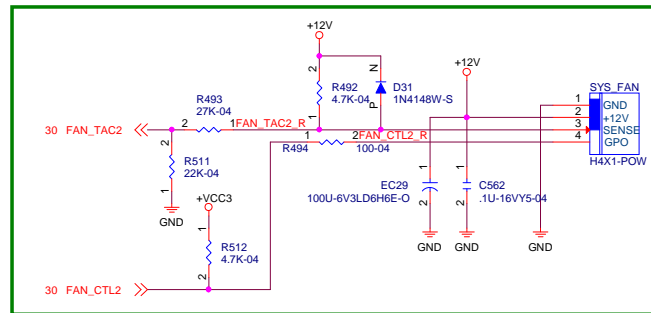
BIOS WP



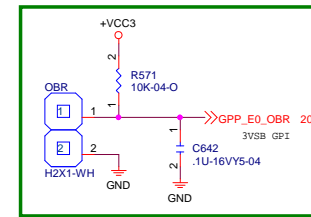
	Ra	Rb	Rc	Rd	Re
A3-A5	O	O	O	O	X
MP	X	X	X	X	O



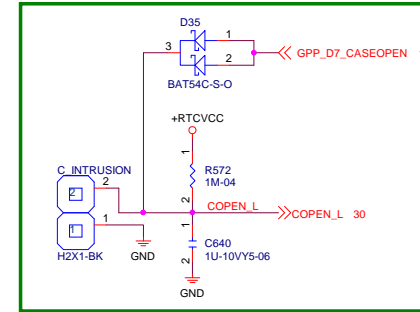
CPU_FAN 4 pin circuit



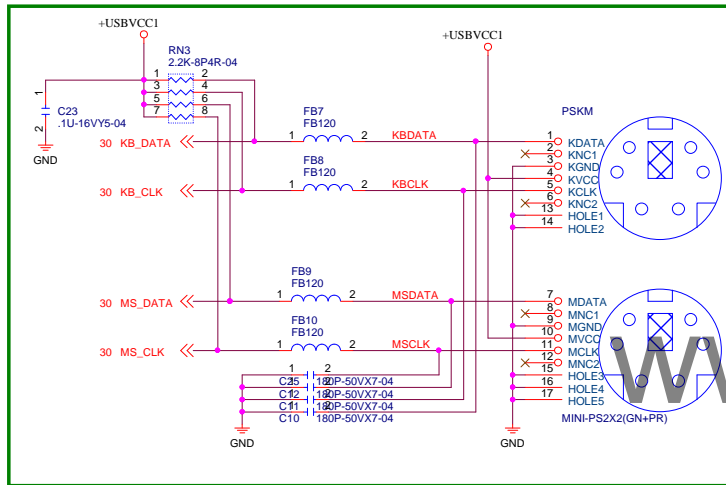
SYS_FAN 4 pin circuit



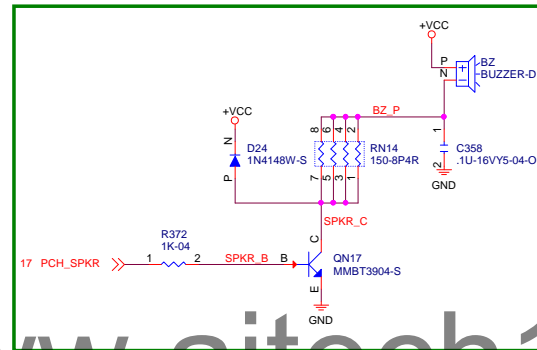
OBR header



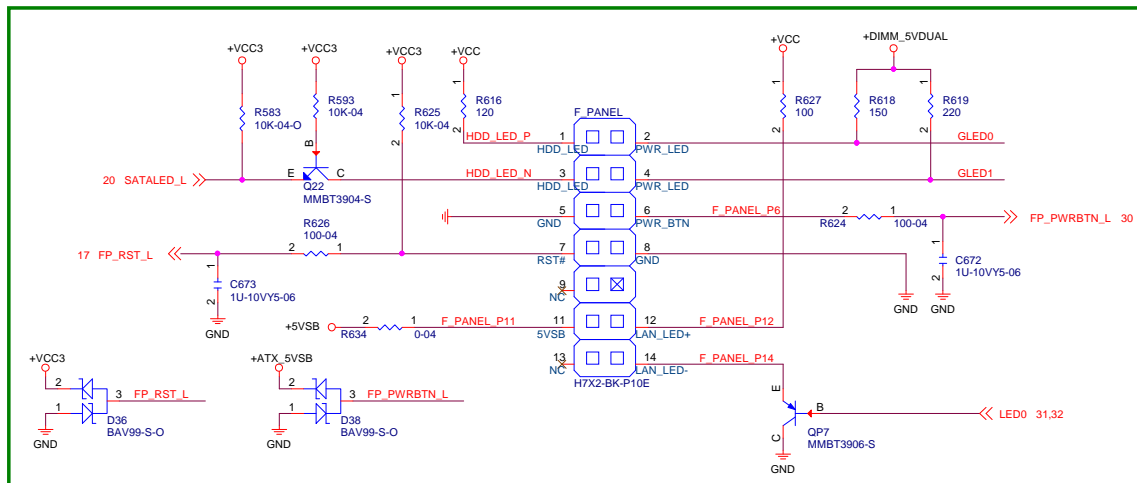
Case open circuit



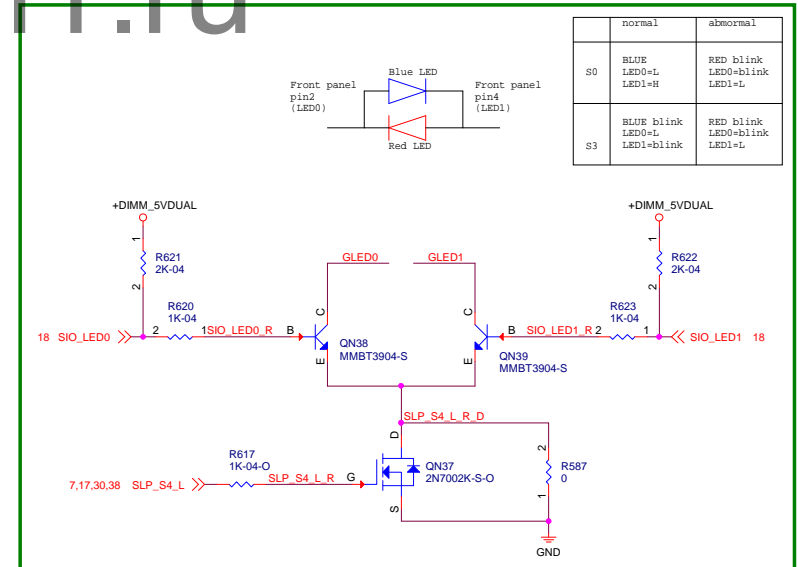
PS2 circuit



Buzzer circuit



Front Panel circuit

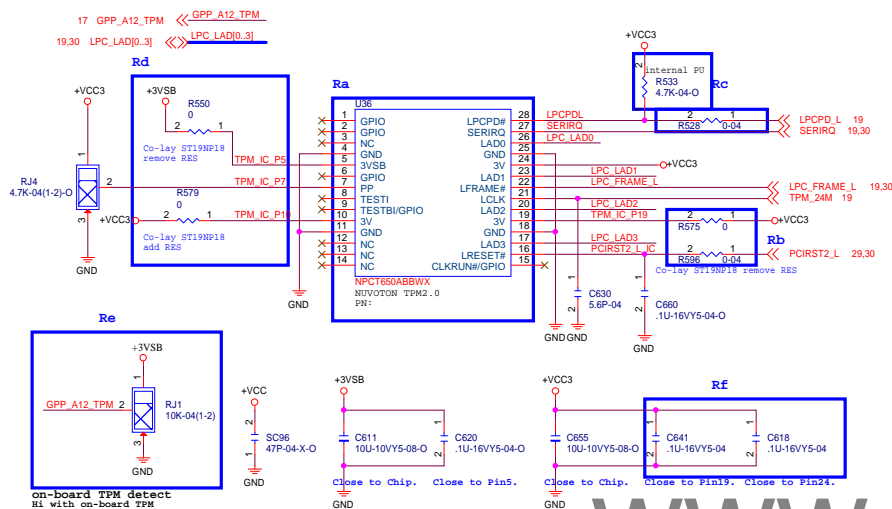


Power LED circuit

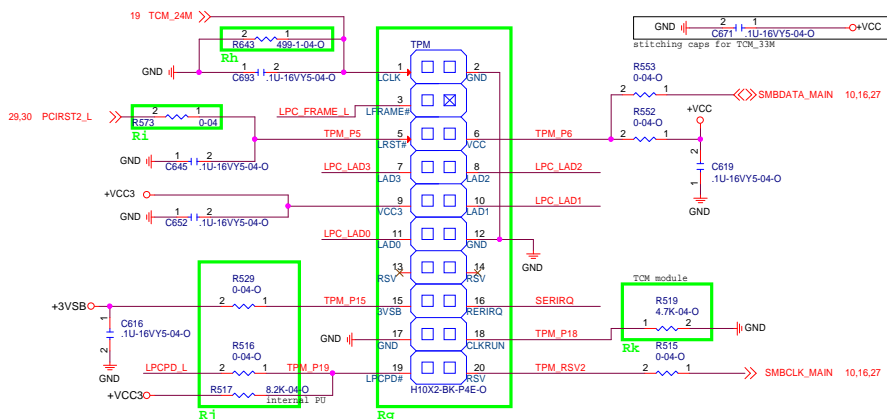
Elitegroup Computer Systems			
Title	FAN/PS2/Buzzer/F_Panel		
Size	Custom	Document Number	Q27H4-AD
Date:	Monday, December 19, 2016	Sheet	28 of 47
Rev	V1.0		

TPM chip/header circuit

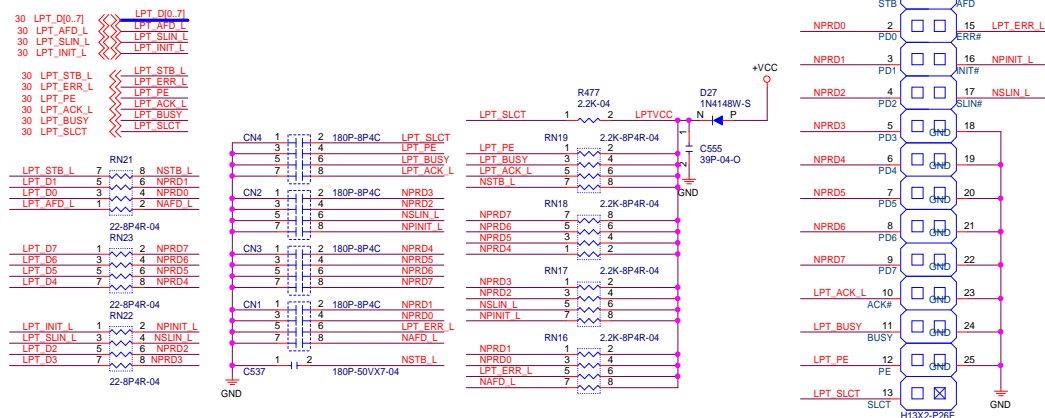
Ra-Rf IC						Rg-Rk Header					
Q170	Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer	O	O	O	O	(1-2)	O	X	X	X	X	X
B150	Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer Founder	X	X	X	X	(2-3)	X	O	O	O	O	O



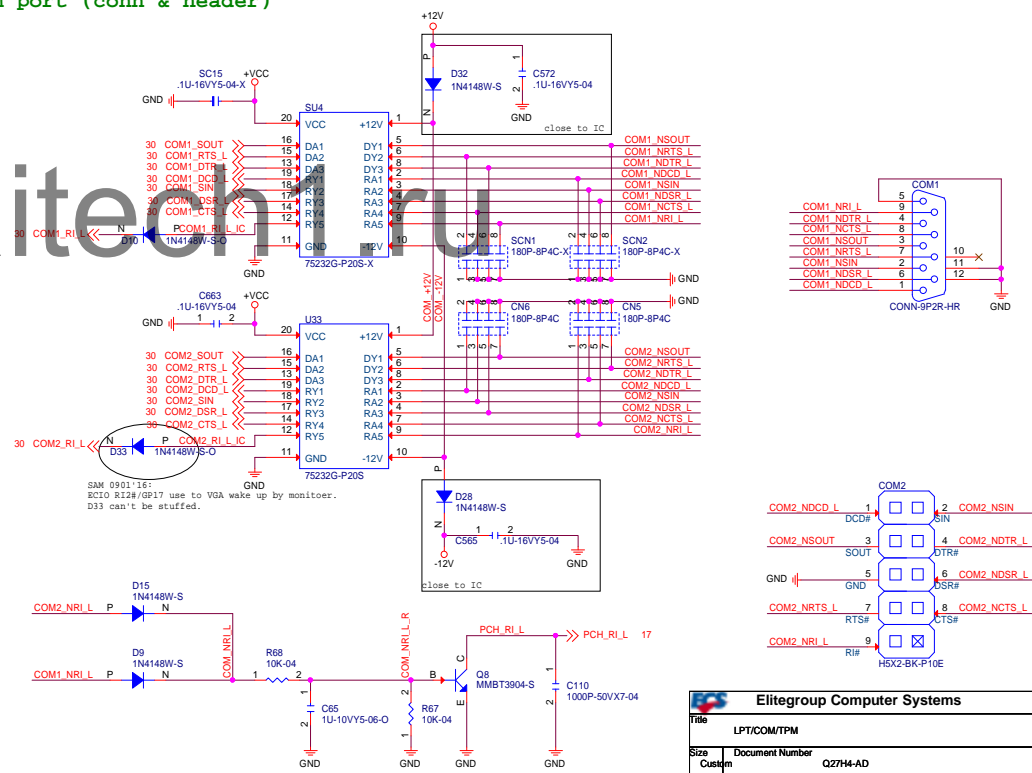
For B150

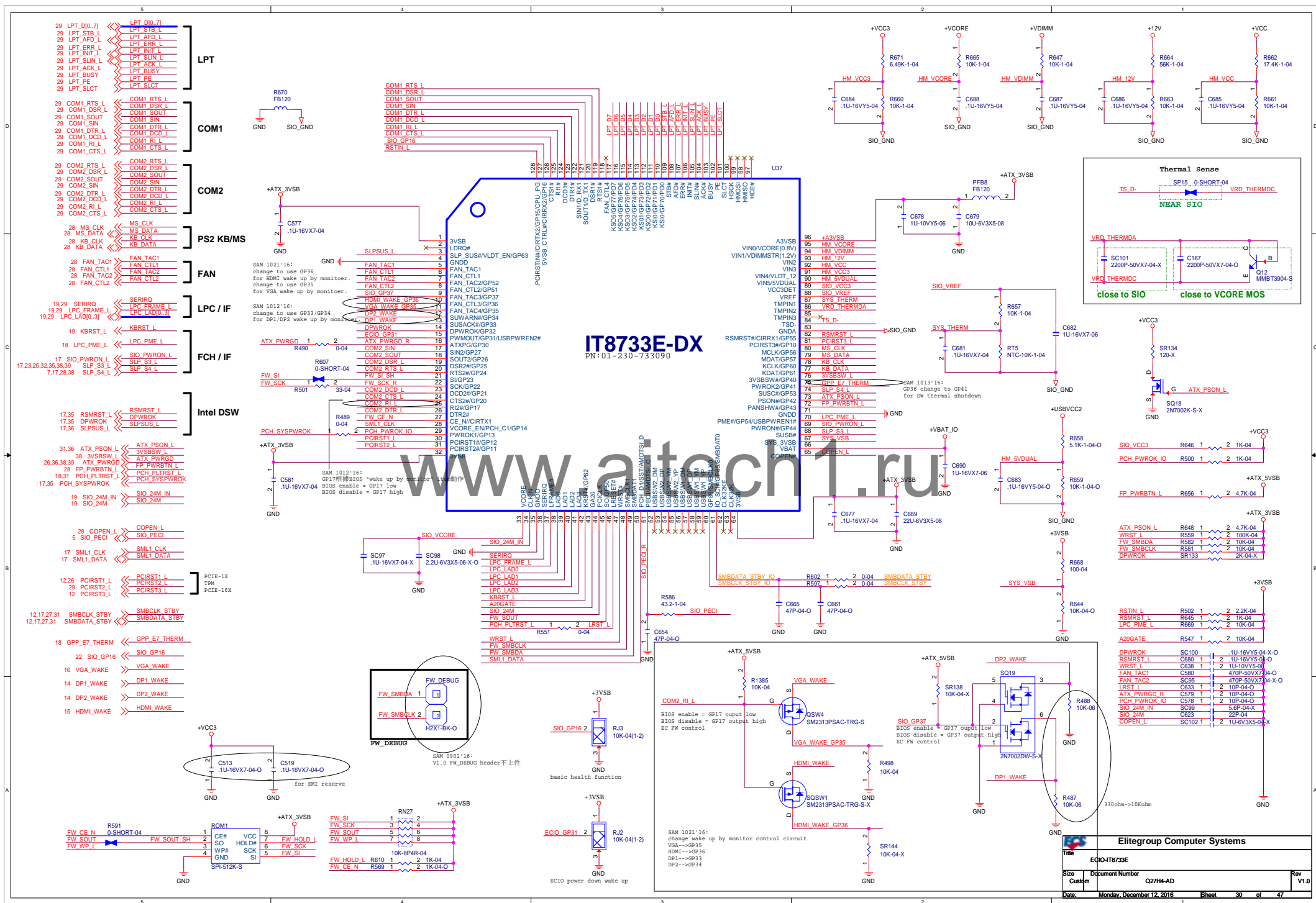


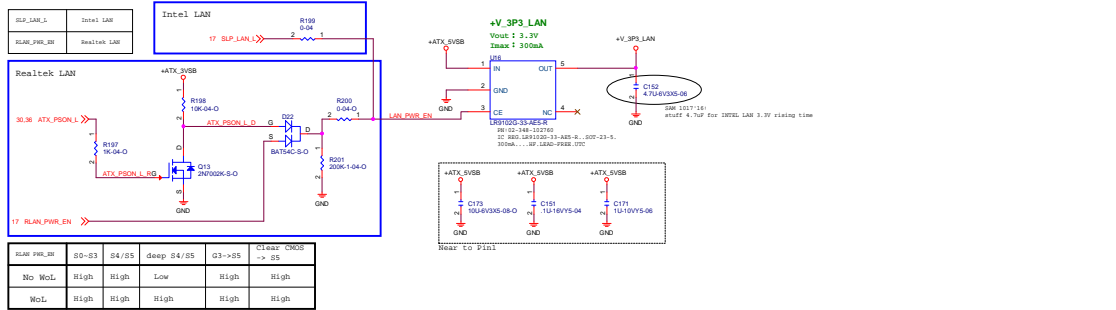
LPT Header



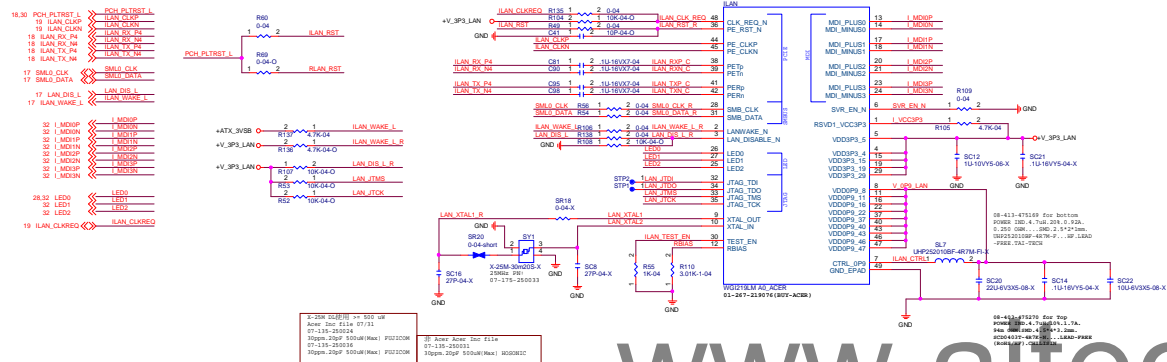
COM port (conn & header)



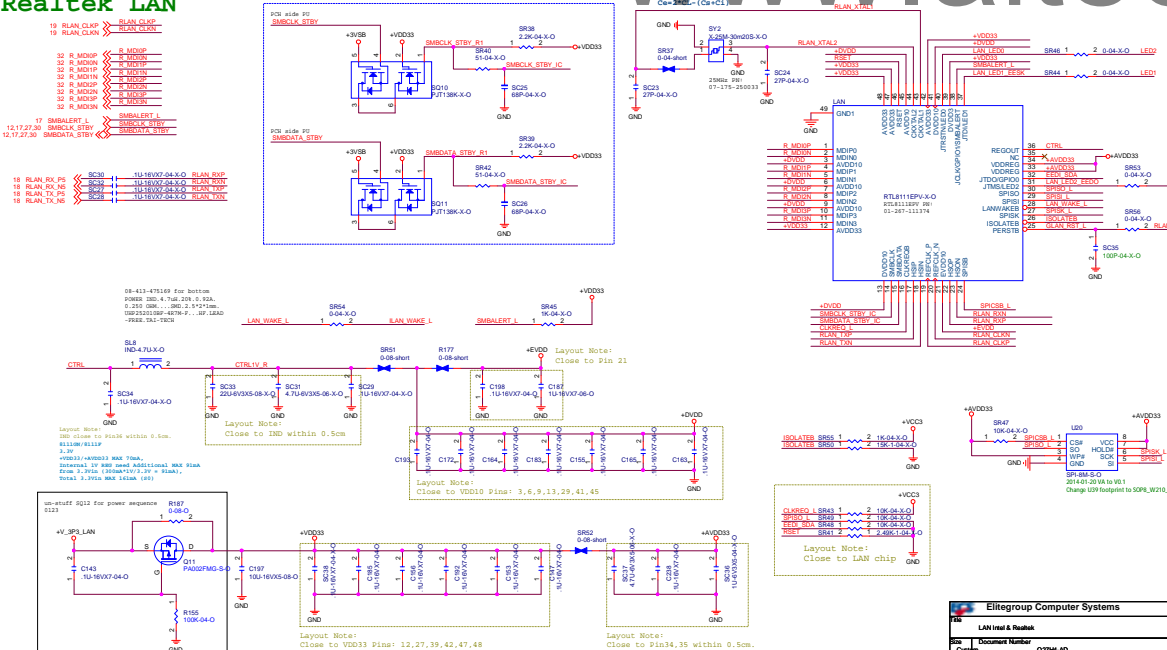


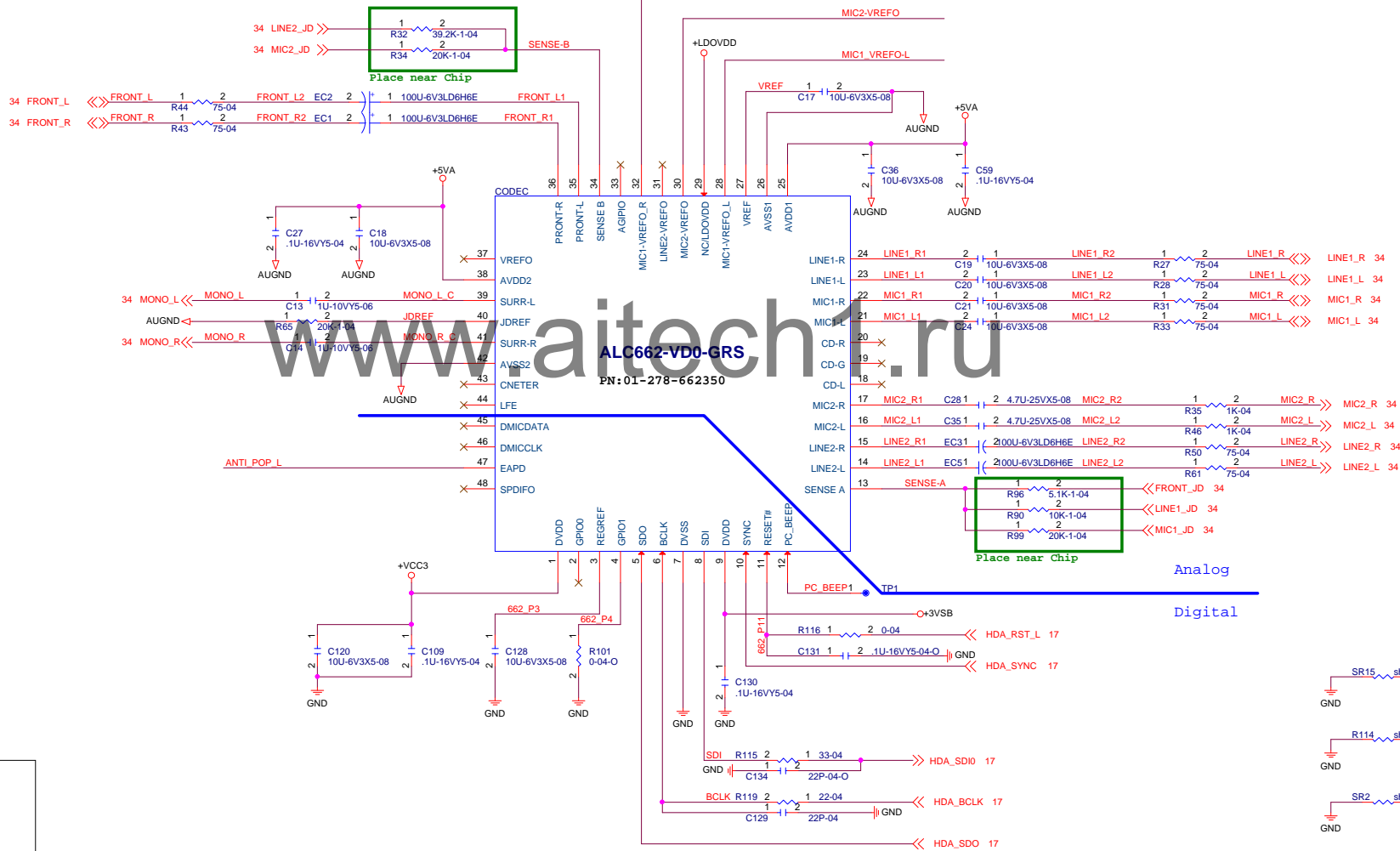
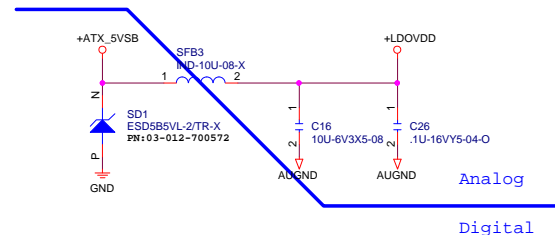
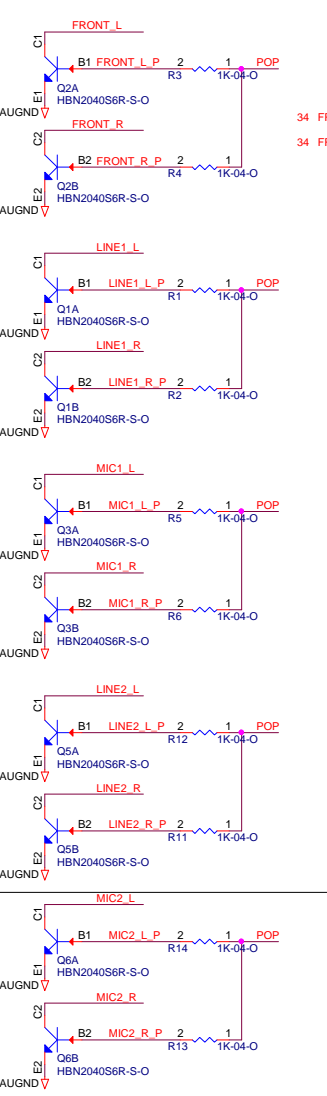


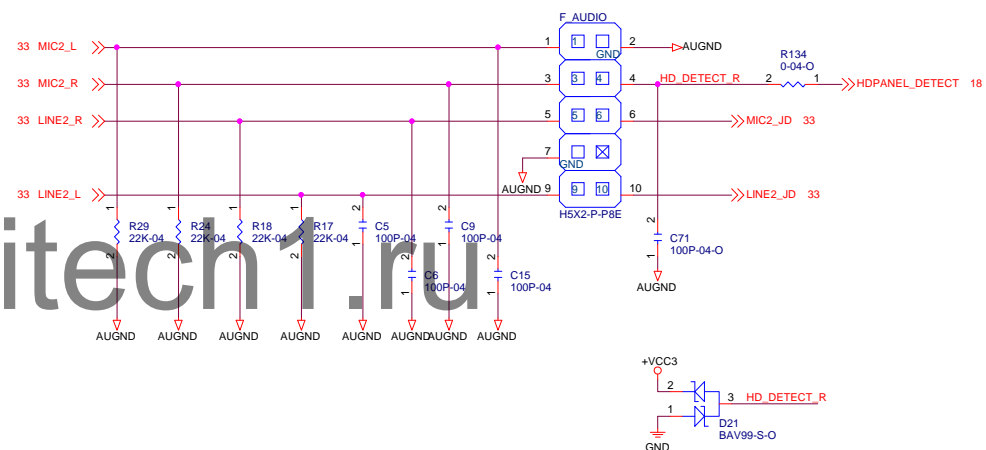
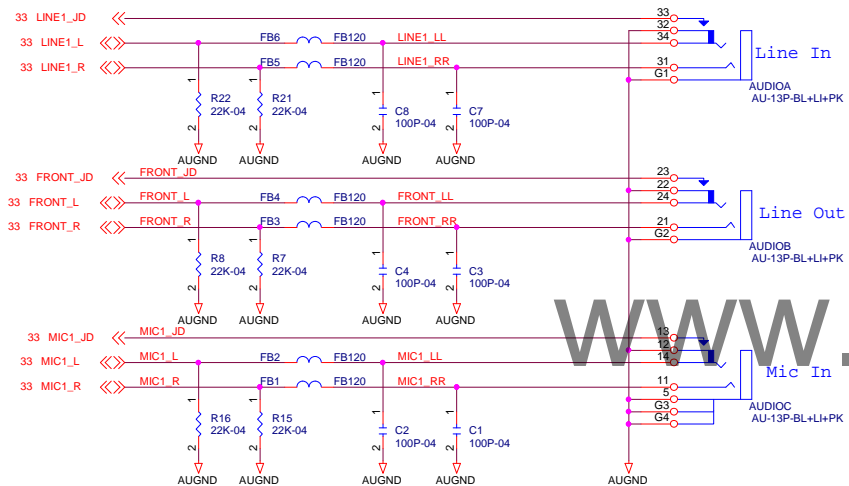
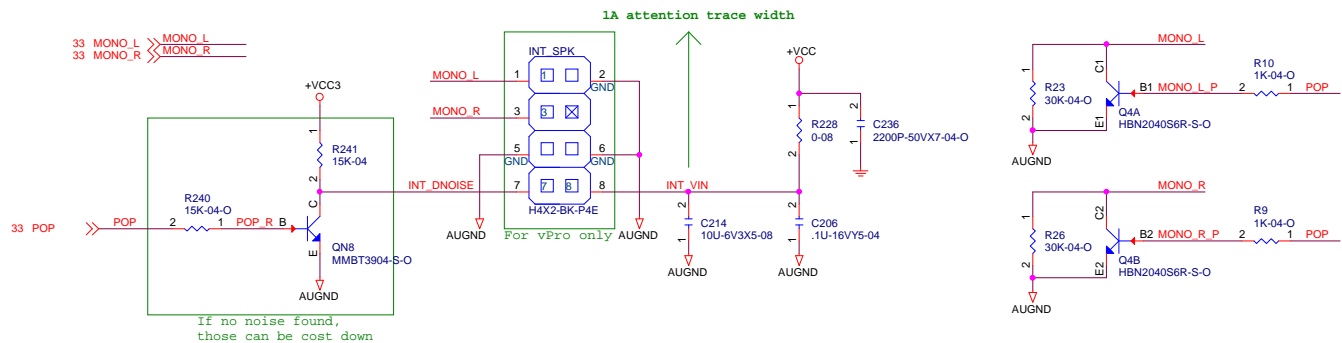
Intel LAN



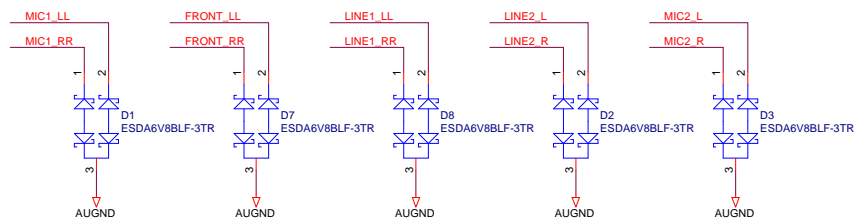
Realtek LAN





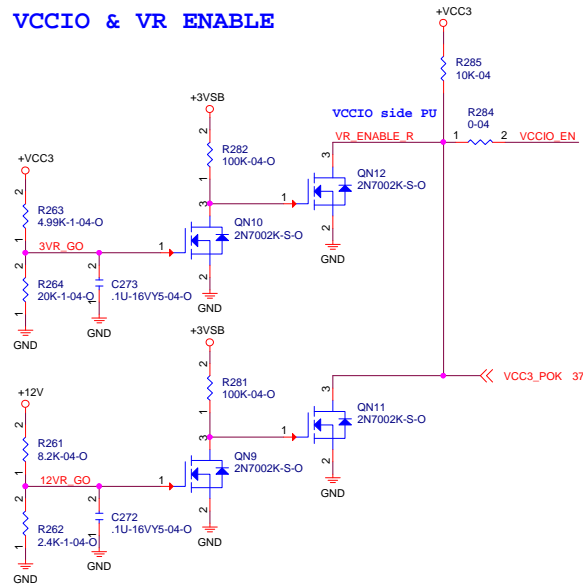


A	B	C
1	LINE IN	LINE IN
2	LINE OUT	LINE OUT
3	MIC IN	MIC IN
4	MIC IN	MIC IN
5	MIC IN	MIC IN

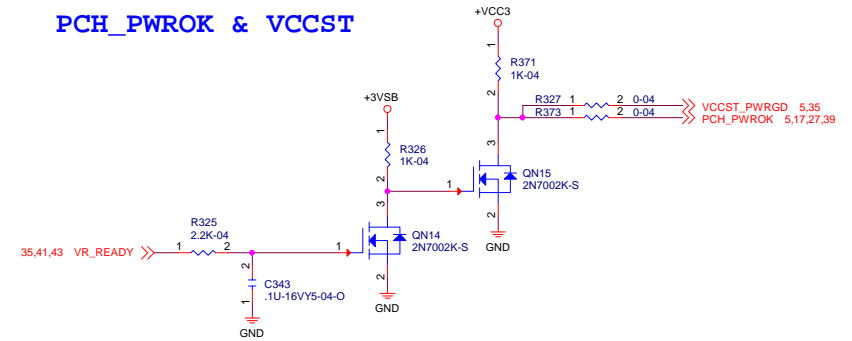


PN:03-100-700872
TVS ARRAY..ESDA6V8BLF-3/TR...SOT-23.5V...LEAD-FREE(RoHS/HF).WILLSEMI

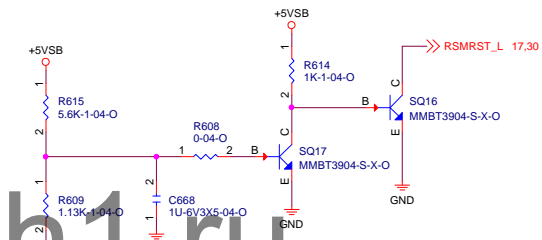
VCCIO & VR ENABLE



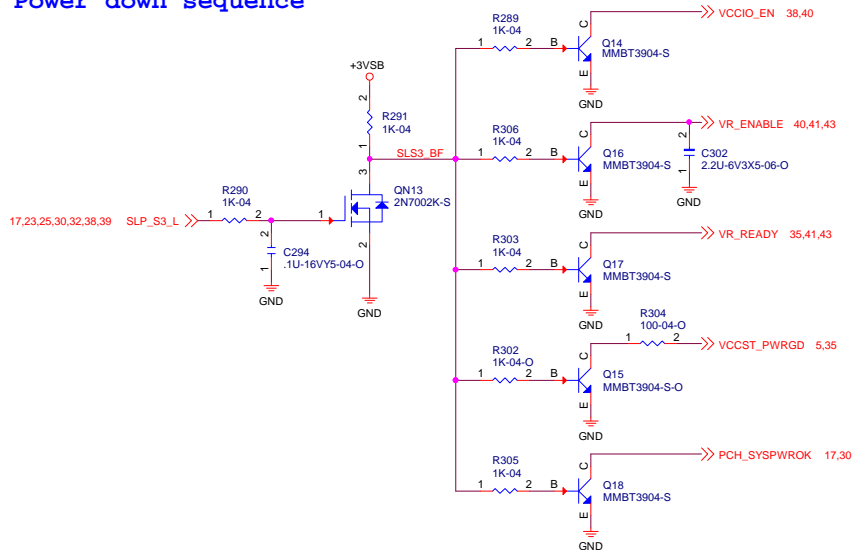
PCH_PWROK & VCCST



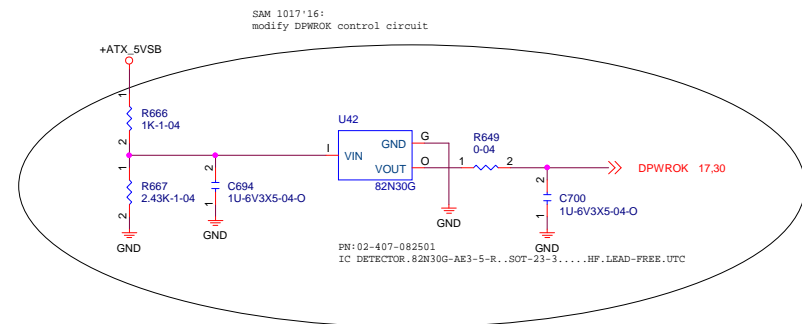
RSMRST#



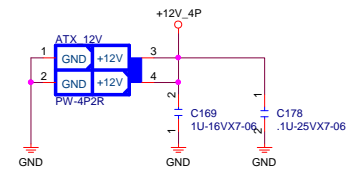
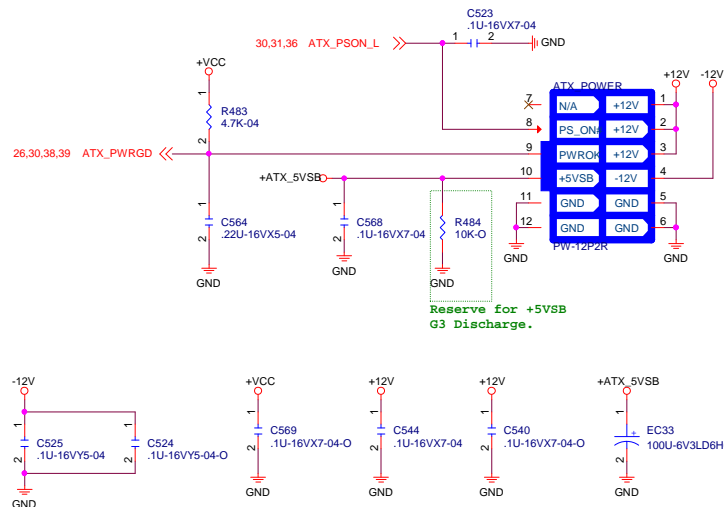
Power down sequence



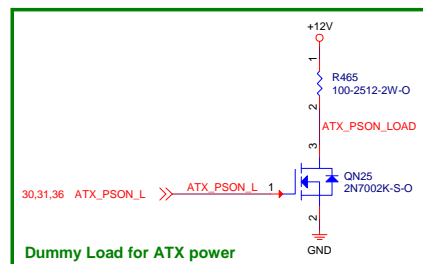
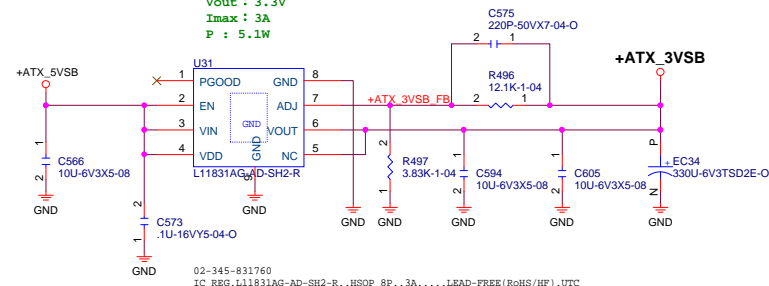
DPWROK



Elitegroup Computer Systems			
Title			
SEQUENCE circuit			
Size	Document Number	Rev	
Custom	Q27H4-AD	V1.0	
Date:	Friday, October 28, 2016	Sheet	35 of 47

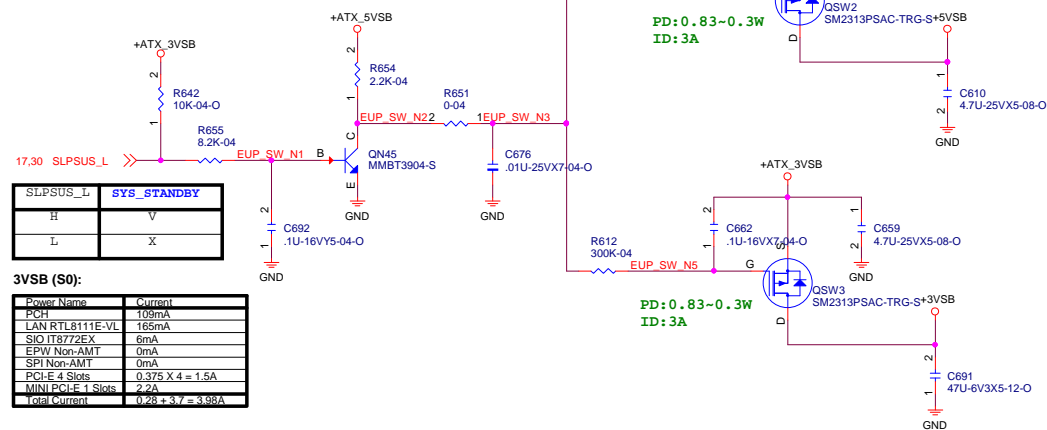


+ATX_3VSB
Vout : 3.3V
Imax : 3A
P : 5.1W



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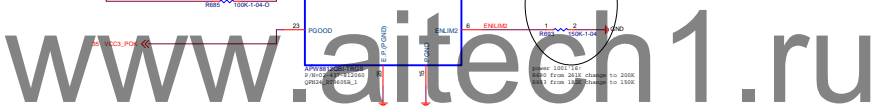
EuP Lot6 Power Saving Circuit



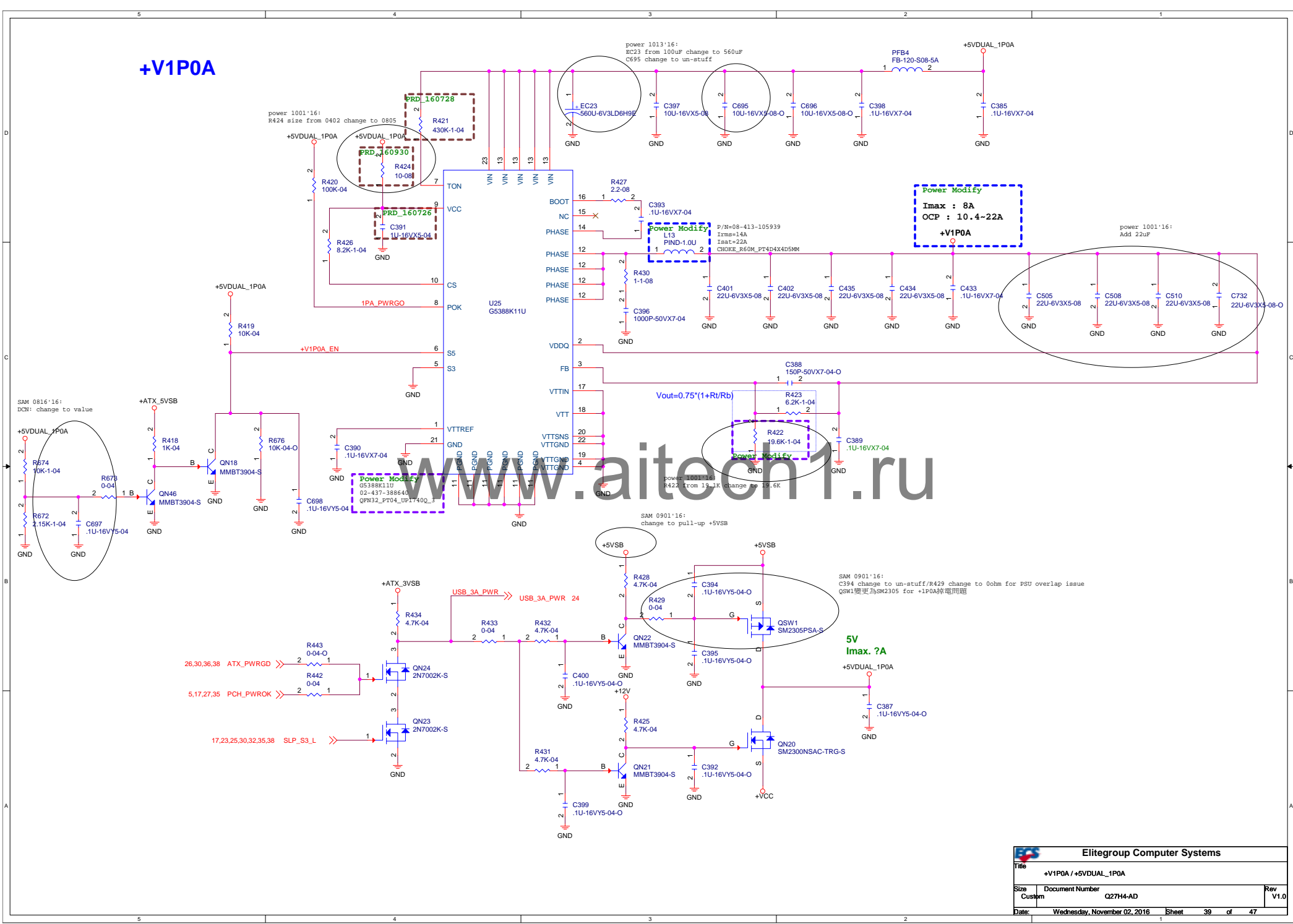
SLPSUS_L	SYS_STANDBY
H	V
L	X

3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A



Title			
+VCC / +VCC3			
Size	Document Number	Rev	
Customer	C277H-A0	V1.0	
Date	Friday, October 28, 2016	Sheet	37 of 47



power 1001'16:
R126 size from 0402 change to 0805

35,41,43 VR_ENABLE << VR_ENABLE

35,38 VCCIO_EN >> VCCIO_EN

Power Modify
G5388K11U
02-437-388640
QPR32_PT04_UP1740Q_3

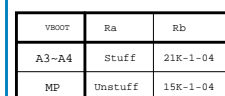
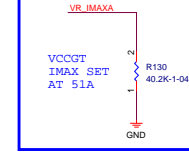
$$V_{out} = 0.75 \cdot (1 + R_t/R_b)$$

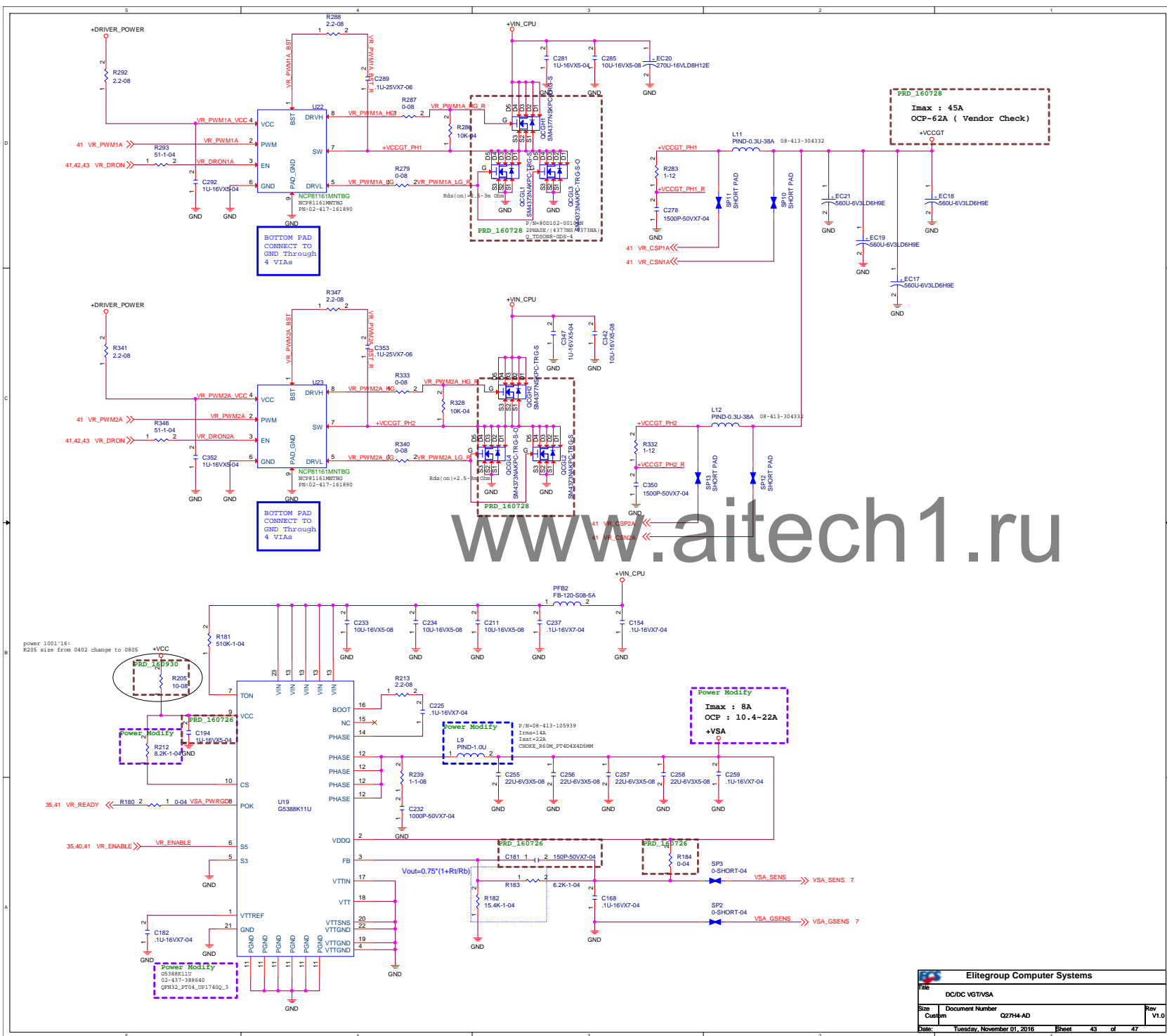
Power Modify
R168
23.2K-1-04

Power Modify
Imax : 5.5A
OCP : 7.2-22A

EE check sequence

Elitegroup Computer Systems			
Title	+VCCIO		
Size	Document Number	Rev	
Custom	Q27H4-AD	V1.0	
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ATX SINGLE P/S		
5VSB +/-5%	12V +/-5%	-12V

ATX4P	
12V +/-5%	



Intel Sky/Kaby Lake CPU			
VCORE	SVID	79A (65W)	
VCC_GT	SVID	45A	
VCC_SA	0.95V	11.1A	
VCCIO	0.95V	5.5A	
VDIMM	1.2V	2.8A	(Iccmax)

DDR4 DIMM	
VDIMM	11A (TDC)
VDIMM_VTT	1A
VPP	2.24A

Intel PCH-H (Q270/B250)			
		S0(A)	Sx(mA)
VCCPRIM_1p0	1V	6.01A	87.4
VCCCLK1	1V	0.035A	0.194
VCCCLK2	1V	0.204A	0.645
VCCCLK3	1V	0.057A	0.22
VCCCLK4	1V	0.036A	0.363
VCCCLK5	1V	0.01A	1.38
VCCMPHY_1p0	1V	3	4
VCCHDAPLL_1p0	1V	0.033A	0.481
VCCAMPHYPLL_1p0	1V	0.08A	0.55
VCCAPLLEBB_1p0	1V	0.075A	0.15
VCCMIPIPLL_1p0	1V	0.036A	0.2
VCCUSB2PLL_1p0	1V	0.012A	0.983
VCCPGPPA	3.3V	0.082A	1.47
VCCPGPPBCH	3.3V	0.229A	0.92
VCCPGPPD	3.3V	0.078A	0.93
VCCPGPEF	3.3V	0.114A	0.6
VCCPGPPG	3.3V	0.065A	0.624
VCCSPI	3.3V	0.029A	0.432
VCCATS	3.3V	0.007A	0.158
VCCHDA	3.3V	0.075A	0.05
VCCPRIM_3p3	3.3V	0.171A	0.543
VCCDSW_3p3	3.3V	0.204A	3.41
VCCRTCPRIM_3p3	3.3V	0.35mA	0.227
VCCRTC	3.0V	0.35mA	0.065

table 10-6

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Icc (mA)	Details
700	All HSIO disabled. Assumes DM1 x4 Running 100%.
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GPIO Port

3VDUAL	
+3VSB	+VCC3

M.2 Slot per key E	
wireless	
VCC3 2A(S0)	3VSB

Total 1 Slots

FAN			
CPU_FAN	+12V	1A	
SYS_FAN	+12V	1A	

+12V

+12V

X16 PCIe Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

X1 PCIe Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

Total 1 Slots

SATA power per	
12V	1A
5V	1A

Total 2 connector

front USB3.0 power switch GS7607SO-RS	
each USB3.0	5VDual 0.9A
PS/2	5VDual 275mA

Total 4 port

front USB3.0 power switch GS7615STDK-R	
each USB3.0	5VDual 1.5A+0.9A

Total 2 port

USB2.0 power switch GS7605ST-RS	
each USB2.0	5VDual 0.5A

Total 5 port

LAN Jacksonville I219LM		
VDD3P3	3.3V	164mA

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	11mA
AVDD	5V	42mA
Internal LDO		

SIO IT8733		
3VSB	3.3V	14mA
VCC3	3.3V	TBD
VBAT	3.3V	2uA

LAN RTL8111EPV		
VDD3P3	3.3V	270mA

Elitegroup Computer Systems			
Title	Power Delivery		
Size	Custom	Document Number	Q27H4-AD
Date:	Monday, December 19, 2016	Sheet	44 of 47
		Rev	V1.0

History

Rev	Date	Notes
A	0901	01.CPU steel's reference from "CPU1" change to "CPU"(P08) 02.F1's footprint change to 0805 & BOM keep using 0805 fuse(P14) 03.wrong net name: change net name to "DONGLE_DP2" on QN4 pin G(P14) 04.SR97 change to stuff 2-3pin, R417 open ME_DISABLE header/jumper change to un-stuff for ME diasable by SW(P17) 05.un-stuff ME_TEST header(P17) 06.R406 stuffed 33ohm for debug card display(P19) 07.C674 change to open & R611 change to 0ohm & R628 change to pull-up +5VSB. U38 use GS7615STDK / G517G1TO1U(P24) 08.stuffed SBOSS1/SBOSS2 for M2_2 holder(P26) 09.C597 stuffed 0.1uF(P36) 10.C713/C721 stuffed 4.7uF(P37) 11.change R485 connection & stuff 10Kohm(P38) 12.C394 change to un-stuff & R429 change to 0ohm & R428 change to pull-up +5VSB(P39) 13.Z1/SZ1 change to use SHORT PAD footprint(P42) 14.For VGA H/Vsync undershoot issue, the damping is changed to 47ohm(P16)
	1001	power change item: 1.C717/C707/C710/C712 change to use 6.3V R690 from 261K change to 200K R693 from 182K change to 150K(P37) 2.R549變更為0805用料,R520 change to 9.53K(P38) 3.R424變更為0805用料,R422變更為19.6K ADD C505/C508/C510 22uF MLCC(P39) 4.R126變更為0805用料(P40) 5.R205變更為0805用料(P43)
	1003	1.SPEC change: DVI-D change to HDMI(P15) 2.SPEC change: power on by monitor (P30)

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Features	Z270	H270	B250	Q250	Q270
Intel® Rapid Storage Technology	Full Features ¹	Full Features ¹	AHCI Mode	AHCI Mode	Full Features ¹
Total USB 3.0 Ports	Up to 10	8	6	8	Up to 10
Total USB 2.0 Ports	14 ³	14 ³	12 ²	14 ³	14 ³
Total SATA 6 Gb/s (Gen3) Ports	Up to 6	Up to 6	Up to 6	Up to 6	Up to 6
Total PCI Express* 3.0 Lanes	Up to 24	Up to 20	Up to 12	Up to 14	Up to 24
Total Controllers for Intel® RST for PCIe* Storage Devices	3 ⁵	2 ⁴	1	1	3 ⁵
Processor PCI Express* 3.0 Lanes Configuration Support	1x16 or 2x8 or 1x8+2x4	1x16	1x16	1x16	1x16 or 2x8 or 1x8+2x4
Processor Over-clocking	No	No	No	No	Yes

HSIO Multiplexing on KBL PCH-H

[illegible]

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Z270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 2.0/PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
H270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe*	PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
B250	USB 3.0/OTG	USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0	N/A	N/A	N/A	LAN Only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q250	USB 3.0/OTG	USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0	USB 2.0	N/A	LAN Only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q270	USB 2.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 2.0/PCIe*	USB 2.0/PCIe*	USB 2.0/PCIe*	USB 3.0/PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*

SKU	15 ¹	16 ³	17	18	19 ¹	20 ¹	21	22	23	24	25	26
Z270 (See Note 2)	PCIe*/ LAN / SATA6a	PCIe*/ SATA1a	PCIe*	PCIe*/ LAN	PCIe*/ LAN / SATA6b	PCIe*/ SATA1b	PCIe*/ SATA2	PCIe*/ SATA2	PCIe*/ SATA4	PCIe*/ SATA5	PCIe*	PCIe*
H270 (See Note 2)	PCIe*/ LAN / SATA6a	PCIe*/ SATA1a	PCIe*	PCIe*/ LAN	PCIe*/ LAN / SATA6b	PCIe*/ SATA1b	PCIe*/ SATA2	PCIe*/ SATA3	SATA4	SATA5	PCIe*	PCIe*
B250	PCIe*/ LAN / SATA6a	PCIe*/ SATA1a	PCIe*	PCIe*/ LAN	SATA6b	SATA1b	SATA2	SATA3	SATA4	SATA5	N/A	N/A
Q250	PCIe*/ LAN / SATA6a	PCIe*/ SATA1a	PCIe*	PCIe*/ LAN	PCIe*/ LAN / SATA6b	PCIe*/ SATA1b	SATA2	SATA2	SATA4	SATA5	N/A	N/A
Q270 (See Note 2)	PCIe*/ LAN / SATA6a	PCIe*/ SATA1a	PCIe*	PCIe*/ LAN	PCIe*/ LAN / SATA6b	PCIe*/ SATA1b	PCIe*/ SATA2	PCIe*/ SATA3	PCIe*/ SATA4	PCIe*/ SATA5	PCIe*	PCIe*

1. Refer to Flexible I/O chapter for the additional information.
2. Only the highlighted (in bold text) PCIe[®] lanes are capable of supporting the Intel[®] RST for PCIe[®] Storage (remapping), configured as x2 or x4.

SKU	27	28	29	30
Z270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
H270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
B25 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
Q250 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*
Q270 (see Note 2)	PCIe*	PCIe*	PCIe*	PCIe*

Note: All PCIe® lanes on H510 27 - 30 are capable of supporting the Intel® RST for PCIe® Storage Device, configured as x2 or x4.